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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
YOR9-2000-0174
Total Pages in this Submission

07/07/00

JC685 U.S. PTO

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

SELF-ALIGNED GATE MOSFET WITH SEPARATE GATES

JC675 U.S. PTO
09/612260
07/07/00

and invented by:

Guy M. Cohen
Hon-Sum Philip Wong

If a **CONTINUATION APPLICATION,** *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: ______

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: ______

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: ______

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having 27 pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

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Docket No. YOR9-2000-0174
Total Pages in this Submission

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   - a. ☒ Formal Number of Sheets 24 (Figs. 1-49)
   - b. ☐ Informal Number of Sheets
4. ☒ Oath or Declaration
   - a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   - b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   - c. ☒ With Power of Attorney ☐ Without Power of Attorney
   - d. ☐ *DELETION OF INVENTOR(S)*
     Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   - a. ☐ Paper Copy
   - b. ☐ Computer Readable Copy *(identical to computer copy)*
   - c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing

    ☐ First Class ☐ Express Mail *(Specify Label No.)*: ____________

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)	Docket No. **YOR9-2000-0174**
(Only for new nonprovisional applications under 37 CFR 1.53(b))	Total Pages in this Submission

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	43	- 20 =	23	x	$18.00	$414.00
Indep. Claims	4	- 3 =	1	x	$78.00	$78.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE ***(specify purpose)***	Assignment Recordation					$40.00
					TOTAL FILING FEE	$1,222.00

☒ A check in the amount of **$1,222.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **50-0481** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Frederick W. Gibb, III
Registration No. 37,629
Customer No. 21254

Dated: July 7, 2000

cc:

Docket No. YOR9-2000-0174

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Guy M. Cohen et al.

Serial No.: Not Yet Assigned | Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith | Examiner: Unknown

For: SELF-ALIGNED GATE MOSFET WITH SEPARATE GATES

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits and calculation of the filing fee, please amend the above-identified application as follows:

IN THE TITLE:

Please amend the title to read --SELF-ALIGNED GATE MOSFET WITH SEPARATE GATES--.

REMARKS

The above change to the title has been made to more completely describe the invention. No new matter has been added.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,

Frederick W. Gibb, III
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July 7, 2000
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APPLICATION
FOR
UNITED STATES
LETTERS PATENT

APPLICANT: Guy M. Cohen
Hon-Sum Philip Wong

FOR: SELF-ALIGNED GATE MOSFET WITH SEPARATE GATES

DOCKET NO.: YOR9-2000-0174

SELF-ALIGNED DOUBLE GATE MOSFET WITH SEPARATE GATES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to a self-aligned double-gate metal oxide semiconductor (DG-MOSFET), with electrically separated top and bottom gates. Moreover, with the invention, the top and bottom gates may be formed by different materials.

Description of the Related Art

The double-gate metal oxide semiconductor field effect transistor (DG-MOSFET), is a MOSFET having a top and a bottom gate which control the carriers in the channel. The double-gate MOSFET has several advantages over a conventional single-gate MOSFET: higher transconductance, lower parasitic capacitance, avoidance of dopant fluctuation effects, and superior short-channel characteristics. Moreover, good short- channel characteristics are obtained down to 20 nm channel length with no doping needed in the channel region. This circumvents all the tunneling break-down, dopant quantization, and impurity scattering problems associated with channel doping.

Conventional systems have attempted to make a double-gate structure with both top and bottom gates self-aligned to the channel region. However, there is no satisfactory method of achieving this self-aligned structure. Previous efforts generally fall into the following categories. A first, category includes etching silicon (Si) into a pillar structure and depositing gates around it (vertical Field Effect Transistor (FET)). A second, category etches a silicon on insulator (SOI) film into a thin bar, makes the source/drain contacts on both ends of the bar, and deposits the gate material on all three surfaces of the thin Si bar. Another way involves making a conventional single-gate MOSFET, then using bond-and-etch back techniques to form the second gate. A fourth conventional method starts with a thin SOI film, patterns a strip and digs a tunnel under it by etching the buried oxide to form a suspended Si bridge. Then, this method deposits the gate material all around the suspended Si bridge.

There are serious drawbacks in all of the above approaches. For example, the first and second require formation of a vertical pillar or Si bar at a thickness of 10nm and it is difficult to reach this dimension with good thickness control and prevent Reactive Ion Etching (RIE) damage. While in the vertical case (first), it is difficult to make a low series resistance contact to the source/drain terminal which is buried under the pillar. In the lateral case (second), the device width is limited by the Si bar height. In the third case, thickness control and top/bottom gate self-alignment are major problems. In the fourth case, the control over the gate

length is poor, and the two gates are electrically connected and must be made of the same material.

A co-pending application by, K. K. Chan, G. M. Cohen, Y. Taur, H.S. P. Wong, entitle “Self-Aligned Double-Gate MOSFET by Selective Epitaxy and Silicon Wafer Bonding Techniques”, 09/272,297, filed March 19, 1999 (hereinafter “Chan”) incorporated herein by reference, utilizes a method for the fabrication of a double-gate MOSFET structure with both top and bottom gates self-aligned to the channel region. The process circumvents most of the problems discussed above. Yet, the top and bottom gates are still physically connected. This occurs because the gate material is deposited in one processing step as an "all- around the channel" gate.

This may not be desirable in some applications for the following reasons. First, from the circuit design point of view, two electrically separated gates are preferable. Second, the bottom gate and top gate are essentially made of the same material, thus only a symmetric DG-MOSFET may be fabricated. Asymmetric DG-MOSFET in which the bottom gate material is different than the top gate cannot be realized.

Chan discloses forming an "all-around the channel" gate by forming a suspended silicon bridge (the channel) followed by the deposition of the gate material conformally around it. To obtain a good threshold voltage control, the channel thickness should be thinned down to 3-5 nm. It is not clear if such thin

bridges can be processed with a high enough yield. Thus, this may impose a limitation on the process suggested in Chan.

Thus, there is a need for a self-aligning DG-MOSFET that is formed by depositing the top and bottom gates independently. Such a structure would produce many advantages. For example, the independent formation of the gates permits the gates to be electrically separated; to be made of varying materials and thickness, and to provide a structure that is planarized, making it easier to connect the device. In addition, there is a need for a DG-MOSFET which permits the formation of a very thin channel.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a structure and method for manufacturing a double-gate integrated circuit which includes forming a laminated structure having a channel layer and first insulating layers on each side of the channel layer, forming openings in the laminated structure, forming drain and source regions in the openings, removing portions of the laminated structure to leave a first portion of the channel layer exposed, forming a first gate dielectric layer on the channel layer, forming a first gate electrode on the first gate dielectric layer, removing portions of the laminated structure to leave a second portion of the channel layer exposed, forming a second gate dielectric layer on the channel layer, forming a second gate electrode on the second gate dielectric layer,

doping the drain and source regions, using self-aligned ion implantation, wherein the first gate electrode and the second gate electrode are formed independently of each other.

The gate dielectric is typically made of SiO_2 but it can be made of other dielectric materials. Also, the gate dielectric associated with the top gate is independent of the gate dielectric associated for the bottom gate. Thus, the gate dielectrics may be of different thicknesses and materials.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a schematic diagram depicting a portion of the depositions and bonding that are used to fabricate a film stack;

Figure 2 is a schematic diagram depicting a portion of the depositions and bonding that are used to fabricate a film stack;

Figure 3 is a schematic diagram depicting a portion of the depositions and bonding that are used to fabricate a film stack;

Figure 4 is a schematic diagram depicting a portion of the depositions and bonding that are used to fabricate a film stack;

Figure 5 is a schematic diagram depicting a portion of the depositions and bonding that are used to fabricate a film stack;

Figure 6 is a schematic diagram depicting a portion of the depositions and bonding that are used to fabricate a film stack;

Figure 7 is a schematic diagram depicting a cross section along line L-L in Figure 8.;

Figure 8 is a schematic diagram depicting a top view of the DG-MOSFET fabricated according to this invention;

Figure 9 is a schematic diagram depicting a cross section of Figure 10 along line L-L;

Figure 10 is a schematic diagram depicting the top view and the of the DG-MOSFET fabricated according to this invention and the extension of the SOI channel into the source and drain regions by epitaxy;

Figure 11 is a schematic diagram depicting the side-wall spacer;

Figure 12 is a schematic diagram depicting the filling of the source and drain trenches with the source/drain material and its subsequent planarization by CMP;

Figure 13 is a schematic diagram depicting the source and drain recesses;

Figure 14 is a schematic diagram depicting the source and drain recess regions filled with a dielectric material;

Figure 15 is a schematic diagram depicting the etching of the top nitride film;

Figure 16 is a schematic diagram depicting side-wall formation;

Figure 17 is a schematic diagram depicting the structure after the growth of the top gate dielectric;

Figure 18 is a schematic diagram depicting the structure after the deposition of the top gate material and its planarization by CMP;

Figure 19 is a schematic diagram depicting the structure with the nitride hard mask that is used to define the device mesa;

Figure 20 is a schematic diagram depicting a cross section of Figure 19 along line L-L;

Figure 21 is a schematic diagram depicting the structure along line L-L after the mesa etch;

Figure 22 is a schematic diagram depicting the structure along line W-W after the mesa etch;

Figure 23 is a schematic diagram depicting the side-wall along line L-L;

Figure 24 is a schematic diagram depicting the side-wall along line W-W;

Figure 25 is a schematic diagram depicting the structure along line L-L after the mesa etch was continued into the box;

Figure 26 is a schematic diagram depicting the structure along line L-L after the mesa etch was continued into the box;

Figures 27 is a schematic diagram depicting the structure along line L-L and the isolation of the exposed source and drain side-walls by oxidation;

Figure 28 is a schematic diagram depicting the structure along line W-W and the isolation of the exposed source and drain side-walls by oxidation;

Figure 29 is a schematic diagram depicting the structure along line L-L after the bottom nitride film was removed by wet etching;

Figure 30 is a schematic diagram depicting the structure along line W-W after the bottom nitride film was removed by wet etching;

Figure 31 is a schematic diagram depicting the structure along line L-L after the growth of the bottom gate dielectric; the deposition of the bottom gate material; and, its planarization by CMP;

Figure 32 is a schematic diagram depicting the structure along line W-W after the growth of the bottom gate dielectric; the deposition of the bottom gate material; and, its planarization by CMP;

Figure 33 is a schematic diagram depicting the structure along line L-L, after removal of the dielectric from the recessed region of the source drain and the formation of a side-wall;

Figure 34 is a schematic diagram depicting the structure along line W-W, after removal of the dielectric from the recessed region of the source drain and the formation of a side-wall;

Figure 35 is a schematic diagram depicting, along line L-L, the self-aligned source/drain implant;

Figure 36 is a schematic diagram depicting, along line L-L, the self-aligned silicide formation;

Figure 37 is a schematic diagram depicting, along line L-L, the self-aligned silicide formation;

Figure 38 is a schematic diagram depicting, along line L-L, that the recessed source and drain regions are re-filled with a dielectric material;

Figures 39 is a schematic diagram depicting the top view and view along line L-L, of the nitride hard mask that is used for the etching of the excess bottom gate material;

Figure 40 is a schematic diagram depicting the top view along line W-W of the nitride hard mask that is used for the etching of the excess bottom gate material;

Figure 41 is a schematic diagram depicting along line L-L the passivation and planarization of the device by a dielectric deposition and CMP;

Figure 42 is a schematic diagram depicting along line W-W the passivation and planarization of the device by a dielectric deposition and CMP;

Figure 43 is a schematic diagram depicting along line L-L the passivation and planarization of the device by a dielectric deposition and CMP;

Figure 44 is a schematic diagram depicting along line W-W the passivation and planarization of the device by a dielectric deposition and CMP;

Figure 45 is a schematic diagram depicting the contact hole (via) opening used to contact the device source, drain and the top and bottom gates;

Figure 46 is a schematic diagram depicting the contact hole (via) opening and used to contact the device source, drain and the top and bottom gates;

Figure 47 is a schematic diagram depicting the contact hole (via) opening and the metalization used to contact the device source, drain and the top and bottom gates;

Figure 48 is a schematic diagram depicting along line W-W the partially completed structure according to the invention; and

Figure 49 is a schematic top view of the inventive structure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

The following describes the present invention which is a self-aligned double-gate metal oxide semiconductor (DG-MOSFET), with electrically separated top and bottom gates and method for making the same. Moreover, the top and bottom gates comprise different materials.

As depicted in figures 1-6, the invention begins by forming a series of layers. First, the invention forms a thin silicon dioxide 1 (e.g., about 2 nm thick) onto a single crystal wafer 5A, which is referred to as the donor wafer. Second, a layer of silicon nitride 2 (which can be, for example, approximately 100 nm thick) is formed onto the silicon dioxide layer 1. Third, a thick (e.g., approximately 400 nm) silicon dioxide layer 3 is formed onto the nitride layer 2. Fourth, the crystal wafer is bonded to a handle wafer 4. This bonding is performed using standard silicon wafer bonding techniques such as boron etch stop, smartCut, and other

techniques well known to those skilled in the art (for a detailed discussion on bonding techniques see Jean-Pierre Colinge, Silicon-On-Insulator Technology, 2nd Ed, Kluwer Academic Publishers, 1997, incorporated herein by reference). Next, the SOI layer 5 is formed to the required thickness for the MOSFET channel. For example, if the smartCut technique is used then a thin Si layer is transferred from the donor wafer 5A surface onto the handle wafer 4. The transferred Si layer is typically bonded onto an insulating film such as SiO2, and is therefore referred to as silicon-on-insulator (SOI). The thickness of the transferred SOI film is determined by the depth of the hydrogen implant which is part of the smartCut technique. Once the SOI film is transferred onto the handle wafer 4 it can be further thinned by oxidation and stripping. The SOI film thickness is typically monitored by ellipsometry or by x-ray diffraction techniques (see G.M. Cohen et. al, Applied Physics Letters, 75(6), p. 787, August 1999, incorporated herein by reference).

Then, a thin silicon dioxide 6 layer (approximately 2 nm) is formed onto the SOI layer 5. This is followed by the formation of a thick silicon nitride 7 layer (e.g., about 150 nm) onto the silicon dioxide layer 6.

After the first series of layers is completed, the invention etches two regions 8 into the stack of films. As depicted in Figures 7 and 8, etch stops (or other similar control features) are positioned some distance into the buried oxide (BOX) 3. The distance between these two regions will become the length (Lg) of the fabricated MOSFET gate.

This disclosure illustrates the inventive structure and process along different cross-sectional lines for clarity. For example, Figures 7, 9, 11-18, 20, 21, 23, 25, 27, 29, 31, 33-38, 40, 41, 43, 45 and 47 are schematic diagrams cut along line L-L, of the top view of the structure shown in Figures 8 and 9.

The invention begins a series of steps to reshape the etched regions. First, as depicted in Figures 9 and 10, an epitaxial silicon (epi) extension 9 is grown selectively out of the single crystal SOI 5 channel. The epi extension 9 extends into the etched regions 8 and is grown around the entire perimeter of the etched regions. The size of the epi extension 9 is preferably about 50 nm. The extension may also be realized by growth of other alloys such as SiGe, SiGeC or other suitable materials well known to those skilled in the art.

Next, the invention forms side-wall spacers 10 on the side-walls of the etched regions 8, as shown in Figure 11. This is performed by depositing a dielectric (not included in the figures) onto the entire structure. The thickness of this dielectric determines the resultant spacer 10 thickness. The dielectric can also be a composite (e.g. subsequent deposition of oxide and nitride layers) to provide etch selectivity. In a preferred embodiment, reactive ion etching is employed to form side wall spacers 10. Also, isotropic etching (reactive ion etching or wet chemical etching) is performed to remove residues of the spacer dielectric from the exposed silicon extension of the SOI channel.

Then, as shown in Figure 12, the invention forms source/drain regions 11. This is done by first depositing amorphous silicon or poly-silicon 11 into the

etched regions 8. As depicted in Figure 12, the amorphous silicon is deposited until the level of amorphous silicon is higher than the top surface of nitride 7. Second, chemical- mechanical polishing (CMP) is used to planarize the top surface. The CMP process mainly removes amorphous-Si and is selective to nitride 7. Next, as depicted in Figure 13, reactive-ion-etching is used to recess 12 the silicon in the source/drain regions 11. Finally, as shown in Figure 14, a dielectric 13 (such as oxide) is deposited into the recessed regions 12, such that the dielectric fully conforms to the recessed region 12. Subsequently, the dielectric is planarized by CMP.

Also, the invention reshapes the top portion of the structure as shown in Figure 15. This is done by, first, removing the top nitride 7 by wet chemical etching (e.g. hot phosphoric acid). Second, side-walls 14 are formed as depicted in Figure 16. The walls are formed by depositing a dielectric conformally onto the entire structure and then etching the dielectric to form side-walls. The thickness of the dielectric determines the thickness of the side-walls 14. Third, the top sacrificial pad oxide 6 is removed by wet chemical etch (e.g. hydrofluoric acid). Next, a top gate dielectric 15 is grown onto the top surface of the SOI channel 5 as shown in Figure 17. The top gate material 16 (e.g. doped polysilicon or tungsten) is conformally deposited to form the gate electrode as shown in Figure 18. Finally, chemical-mechanical polishing is used to planarize the top surface. The CMP process mainly removes the top gate material using a slurry that is selective to nitride 7.

Subsequently, the invention places a mesa hard mask 17 onto the structure as shown in Figures 19 and 20. The mesa hard mask is comprised of a deposition nitride film which is preferably about 100 nm thick and is subsequently patterned. Figures 22, 24, 26, 28, 30, 32, 42, 44, 46, and 48 are cross-sectional views along line W-W, shown in Figure 19.

More specifically, the invention isolates individual devices using the mesa hard mask 17. The structure is patterned as follows: (1) etching with reactive ion etching (RIE) past the SOI film and stopping on the nitride as shown in Figures 21 and 22; (2) depositing a dielectric such as low temperature oxide (LTO) of preferably about 75 nm conformally on the entire structure and etching the dielectric to form a sidewall 18 as shown in Figures 23 and 24; (3) completing the mesa etch by etching some distance into the BOX 3 as shown in Figures 25 and 26. The sidewall of the bottom nitride 2 is also exposed during this process.

As depicted in Figures 27 and 28, the invention grows a thermal oxide 19 to isolate the exposed source and drain side-wall. Then, as depicted in Figures 29 and 30, the invention removes the bottom nitride 2 and top nitride hard mask 17 by wet chemical etching (e.g., hot phosphoric acid). The removal of the bottom nitride 2 forms a tunnel 20 along the device in the width dimension and a suspended bridge along the length dimension. Also, the bottom sacrificial pad oxide 1 is removed by wet chemical etch (e.g. hydrofluoric add).

Next, as shown in Figures 31 and 32, the invention forms the bottom gate electrode 22. This is done by first growing bottom gate dielectric 21 on the

bottom surface of the SOI channel 5. The bottom gate material 22 (e.g. doped poly- silicon, tungsten, etc.) is conformally deposited to form the bottom gate electrode. Next, CMP is used to planarize the top surface. The CMP process mainly removes the bottom gate material and is selective to the LTO 13.

As shown in Figure 33, the invention etches the source/drain cap dielectric LTO 13. The invention deposits a dielectric conformally on the entire structure to form side-walls 23, as shown in Figure 34. Once again, the thickness of this dielectric determines the resultant spacer thickness. The dielectric is then etched to form the final side-wall structure 23.

Next the invention, dopes source/drain regions 11 using a self-aligned ion-implantation 24 to heavily dope the silicon 11 as shown in Figure 35. To mask the SOI channel region from the ion implantation, the top poly gate 16 is used as a self-aligned implant mask. The side-wall spacer 23 will offset the source/drain implant from the channel region. The implant is followed by a rapid thermal annealing to activate the dopant.

A self-aligned silicide process is then applied to form the silicide 26 over the source/drain and gates 11, as shown in Figure 37. This is accomplished using any standard process well known to those skilled in the art. For example, in preparation for application of the silicide, a metal 25 such as cobalt (Co) or titanium (Ti) is deposited conformally on the entire structure as shown in Figure 36 and the structure is heated. After the silicide is deposited, a dielectric such as LTO is conformally deposited over the silicide to form an LTO cap 27, shown in

Figure 38. This is followed by CMP which is used to planarize the top surface. The CMP process mainly removes the dielectric material 27 and is selective to the silicide 26 and/or the gate materials 16 and 22. Due to a finite selectivity of the CMP process some or all of the gate silicide 26 may be removed. In this case, the self-aligned silicide process may be repeated to form a new gate silicide.

Next, the bottom gate 22 is finalized. First, a nitride or LTO film 27 of preferably about 100 nm is deposited and subsequently patterned by photolithography to form a hard mask that defines the bottom gate area 28 as shown in top view in Figure 39 and cross-section along line L-L in Figure 40. Second, the excess bottom gate material 22 is etched down to the BOX 3, and a thick passivation dielectric is deposited 29 as shown in Figures 41 and 42. CMP is again used to planarize the top surface. The CMP process mainly removes the dielectric material 29 and is selective to not remove the nitride hard mask 28. A second passivation dielectric is then deposited 30 as shown in Figures 43 and 44.

Next, contact holes 31 are formed on the source, and drain 11, and contact holes 32 are etched over the two gates 16, 22, by photo-lithography patterning and etching as shown in Figures 45 and 46. Metalization 33 is then deposited and subsequently patterned to form electrical contacts to the source, the drain, and the bottom and top gates electrodes as shown in Figures 47 and 48. If the gate length is very short, two levels of metalization may be applied to allow for more relaxed design rules for the contact of the top gate. Figure 49 shows a top view of the completed structure.

Many benefits over the prior art are realized by the specific improvements of this invention. First, this invention deposits the top and bottom gates in two separate steps and creates top and bottom gates that are electrically separated, which results in several advantages. For example, the bottom gate may be used to control the threshold voltage, thereby allowing a mix threshold voltage (Vt) circuit for low power applications.

This structure also allows for increases in the circuit density. When gates are electrically separated the double-gate MOSFET comprises a four terminal device with two input gates. Thus, a single device can be used to implement binary logic operations such as a NOR (nFET) or a NAND (pFET) cell. The implementation of these binary logic functions would typically require two standard MOSFETs per cell. This increase in the circuit density also applies to analog circuits. For example a mixer may be implemented by applying the oscillator voltage to one gate and the signal (data) voltage to the other gate.

Since the invention grows the top and bottom gates and respective gate dielectrics independently, the gates and gate dielectrics may be of different materials and different thicknesses. Also different doping levels and doping species may be incorporated into each gate. Thus, asymmetric gates may be fabricated. The asymmetric double-gate MOSFET is most useful for a mixed application where the gates are tied together to achieve speed and can be used separately to achieve low power and high density e.g. for static random access memory (SRAM).

Also, the invention provides a structure that is planar, making it easier to connect the device. Devices with a very thin channel of about 3 to 5 nm thick may be required to obtain a good threshold voltage behavior. Fabricating suspended silicon bridges with a thin layer may reduce the overall yield. This invention supports the channel with a thick layer 22. Thus, the invention allows devices with a very thin channel to be fabricated and permits such devices to obtain a good threshold voltage behavior. The invention also utilizes a self-aligned silicide process which lowers the series resistance.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region;

wherein said first gate and said second gate are electrically separated from each other.

2. The transistor of claim 1, wherein said first gate comprises a different doping concentration that said second gate.

3. The transistor of claim 1, wherein said first gate comprises a different doping species than said second gate.

4. The transistor of claim 1, further comprising a first gate dielectric below said first gate and a second gate dielectric above said second gate.

5. The transistor of claim 1, wherein said first gate has a first conductive contact and said second gate has a second conductive contact and said first conductive contact and said second conductive contact are coplanar.

6. The transistor of claim 1, wherein said first gate comprises a different material than said second gate.

7. The transistor of claim 1, wherein said first gate comprises a different thickness than said second gate.

8. The transistor of claim 1, wherein said first gate, said second gate and said channel region form a planarized structure.

9. The transistor of claim 4, wherein said first gate dielectric comprises a different material than said second gate dielectric.

10. The transistor of claim 4, wherein said first gate dielectric comprises a different thickness than said second gate dielectric.

11. A semiconductor chip having at least one transistor, said transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region;

wherein said first gate comprises a different material than said second gate.

12. The semiconductor chip of claim 11, wherein said first gate and said second gate have

different dopant concentrations.

13. The semiconductor chip of claim 11, wherein said first gate and said second gate have different dopant species.

14. The semiconductor chip of claim 11, further comprising a first gate dielectric below said first gate and a second gate dielectric above said second gate.

15. The semiconductor chip of claim 14, wherein said first gate dielectric comprises a different material than said second gate dielectric.

16. The semiconductor chip of claim 14, wherein said first gate dielectric comprises a different thickness than said second gate dielectric.

17. The semiconductor chip of claim 11, wherein said first gate has a first conductive contact and said second gate has a second conductive contact and said first conductive contact and said second conductive contact are coplanar.

18. The semiconductor chip of claim 11, wherein said first gate and said second gate are electrically separated.

19. The semiconductor chip of claim 11, wherein said first gate and said second gate have

different thicknesses.

20. The semiconductor chip of claim 11, wherein said first gate, said second gate and said channel region form a planarized structure.

21. A method of forming a transistor comprising:

forming a laminate structure including a first gate over a channel region;

removing portions of said laminate below said channel region; and,

forming a second gate below said channel region,

wherein said first gate and said second gate are electrically separated from each other.

22. The method of forming a transistor according to claim 21, wherein said first gate supports said channel region during said removing process.

23. The method of forming a transistor according to claim 21, wherein said first gate comprises a different doping concentration than said second gate.

24. The method of forming a transistor according to claim 21, further comprising applying different doping species to said first gate and said second gate.

25. The method of forming a transistor according to claim 21, further comprising forming a first gate dielectric below said first gate and a second gate dielectric above said second gate.

26. The method of forming a transistor according to claim 24, wherein said first gate dielectric comprises a different material than said second gate dielectric.

27. The method of forming a transistor according to claim 24, wherein said first gate dielectric comprises a different thickness than said second gate dielectric.

28. The method of forming a transistor according to claim 21, further comprising forming a first gate oxide below said first gate and a second gate oxide above said second gate.

29. The method of forming a transistor according to claim 21, wherein said first gate has a first conductive contact and said second gate has a second conductive contact and said first conductive contact and said second conductive contact are coplanar.

30. The method of forming a transistor according to claim 21, wherein said first gate comprises a different material than said second gate.

31. The method of forming a transistor according to claim 21, wherein said first gate comprises a different thickness than said second gate.

32. The method of forming a transistor according to claim 21, wherein said first gate, said second gate and said channel region form a planarized structure.

33. A method of manufacturing a double-gate transistor comprising:

forming a laminated structure having a channel layer and first insulating layers on each side of said channel layer;

forming openings in said laminated structure;

forming drain and source regions in said openings;

removing portions of said laminated structure to leave a first portion of said channel layer exposed;

forming a first gate dielectric on said channel layer;

forming a first gate electrode on said first gate dielectric layer;

removing portions of said laminated structure to leave a second portion of said channel layer exposed;

forming a second gate dielectric layer on said channel layer;

forming a second gate electrode on said second gate dielectric layer;

doping said drain and source regions,

wherein said first gate electrode and said second gate electrode are formed independently of each other.

34. The method in claim 33, wherein, said first and second gate electrode are electrically separated.

35. The method in claim 33, wherein said doping of said drain and source regions comprises

a self-aligned ion implantation.

36. The method in claim 33, wherein said method further comprises forming said first gate electrode to have a thickness and greater than that of said second gate electrode.

37. The method in claim 33, wherein said method further comprises forming said first gate to have a width greater than that of said second gate.

38. The method in claim 33, wherein said method further comprises forming said first gate dielectric to have a width greater than that of said second gate dielectric.

39. The method in claim 33, further comprising forming said first gate from a first material and said second gate from a second material.

40. The method in claim 33, further comprising forming said first gate dielectric from a first material and said second gate dielectric from a second material.

41. The method in claim 33, wherein said removing portions of said laminate structure leaves a second portion of said channel layer exposed, forms a tunnel in said laminate, and,

wherein said tunnel is formed between an upper layer and a lower layer and said lower layer.

42. The method in claim 33, wherein said first gate dielectric comprises a different material than said second gate dielectric.

43. The method of forming a transistor according to claim 33, wherein said first gate dielectric has a different thickness than said second gate dielectric.

SELF-ALIGNED DOUBLE-GATE MOSFET BY SELECTIVE EPITAXY AND SILICON WAFER BONDING TECHNIQUES

ABSTRACT

A structure and method of manufacturing a double-gate integrated circuit which includes forming a laminated structure having a channel layer and first insulating layers on each side of the channel layer, forming openings in the laminated structure, forming drain and source regions in the openings, removing portions of the laminated structure to leave a first portion of the channel layer exposed, forming a first gate dielectric layer on the channel layer, forming a first gate electrode on the first gate dielectric layer, removing portions of the laminated structure to leave a second portion of the channel layer exposed, forming a second gate dielectric layer on the channel layer, forming a second gate electrode on the second gate dielectric layer, doping the drain and source regions, using self-aligned ion implantation, wherein the first gate electrode and the second gate electrode are formed independent of each other.

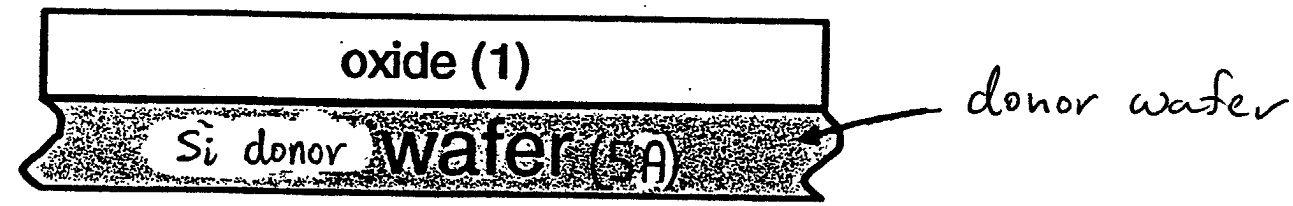


FIGURE 1

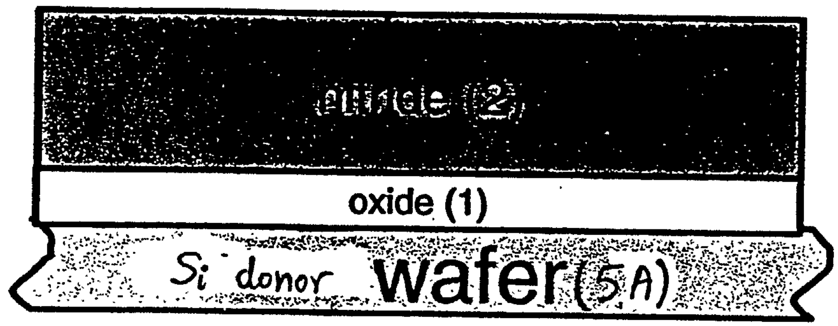


FIGURE 2

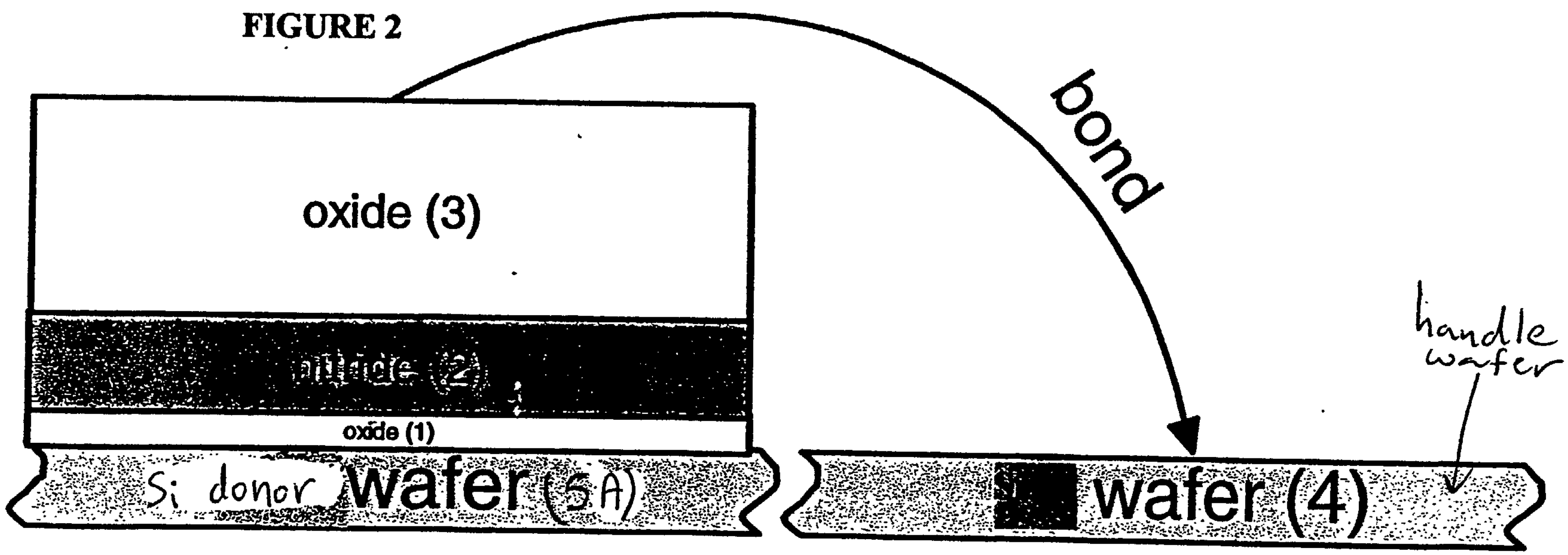


FIGURE 3

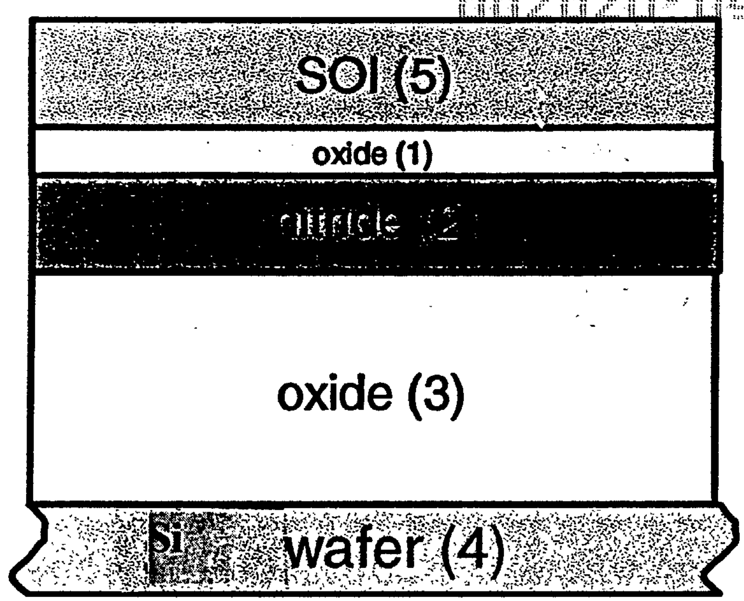


FIGURE4

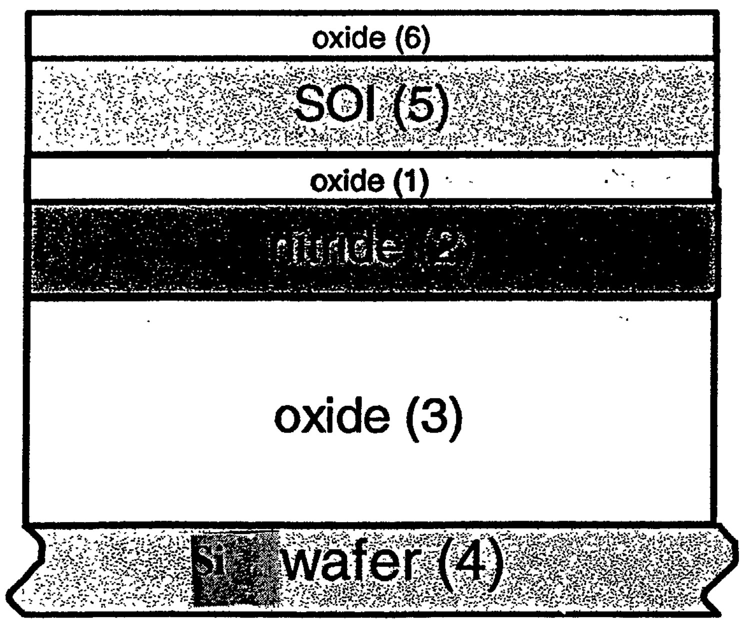


FIGURE 5

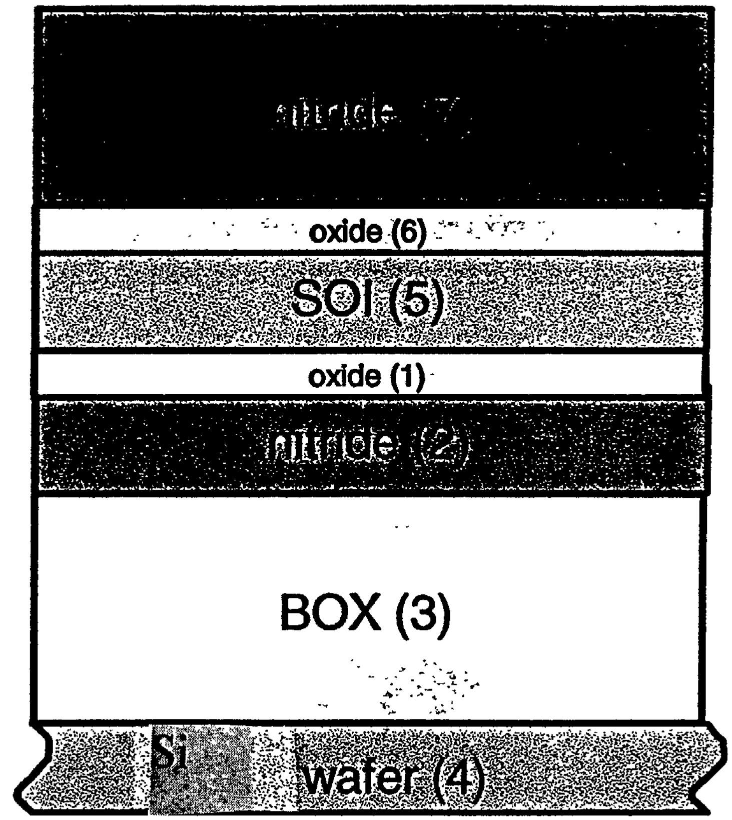


FIGURE 6

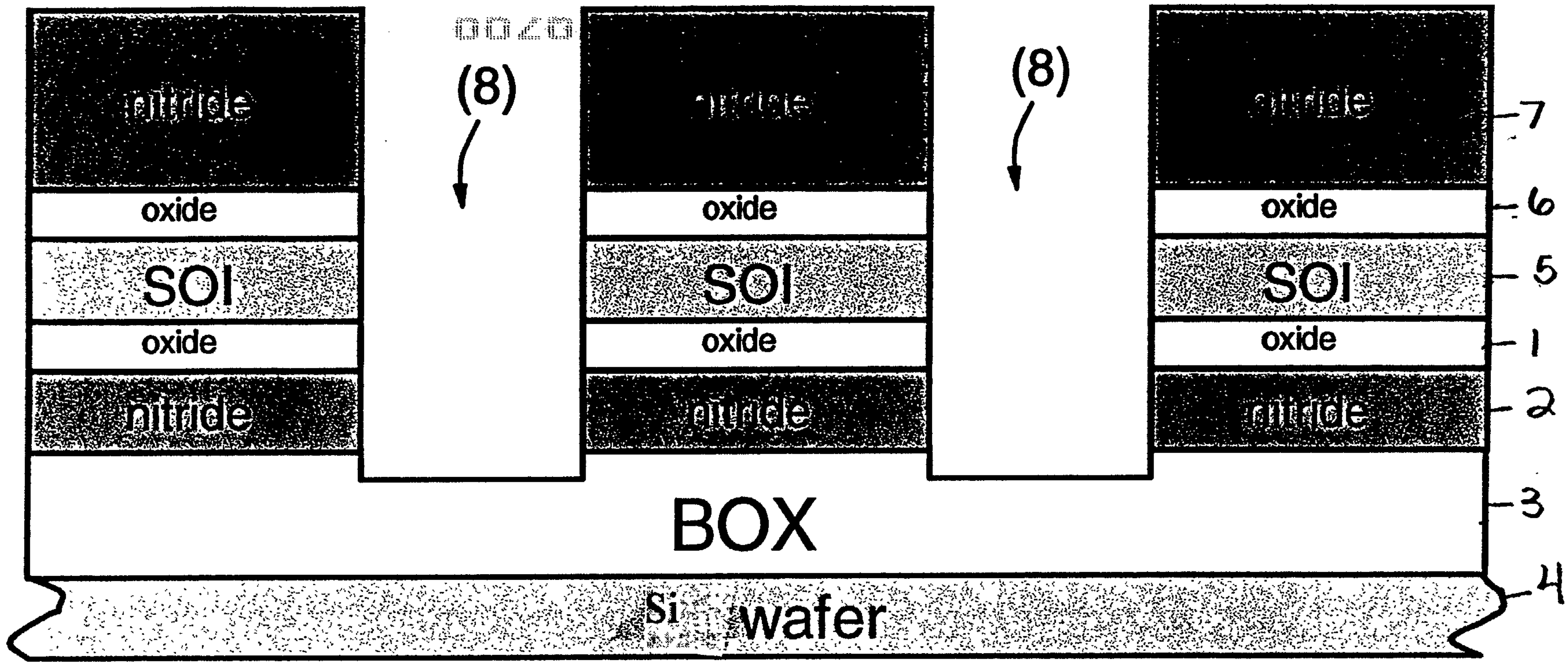


FIGURE 7

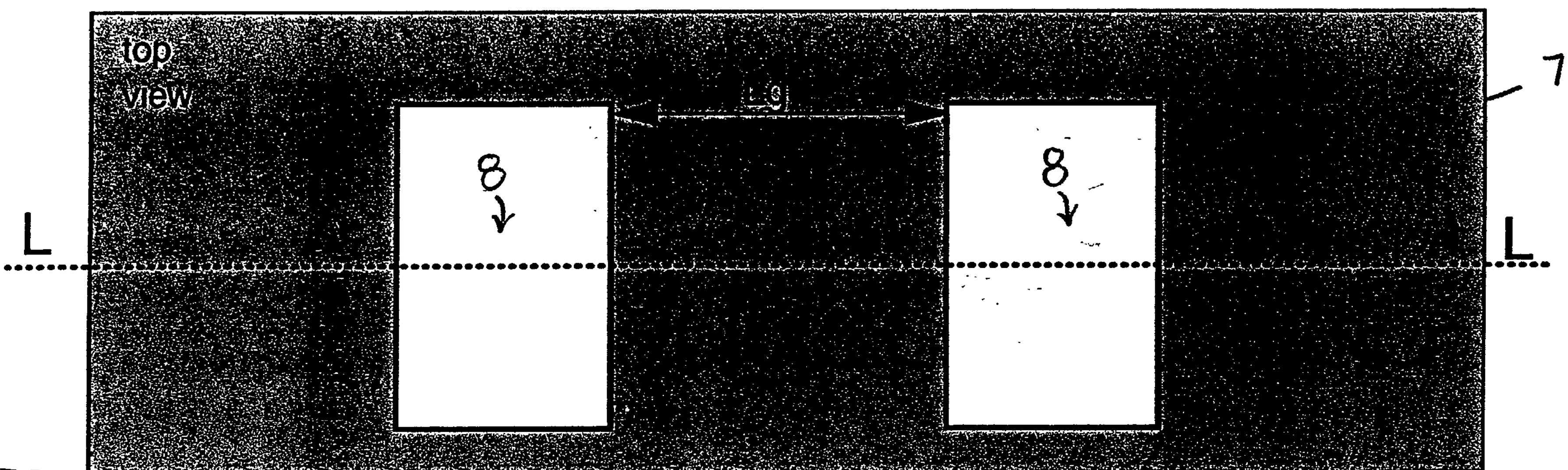


FIGURE 8

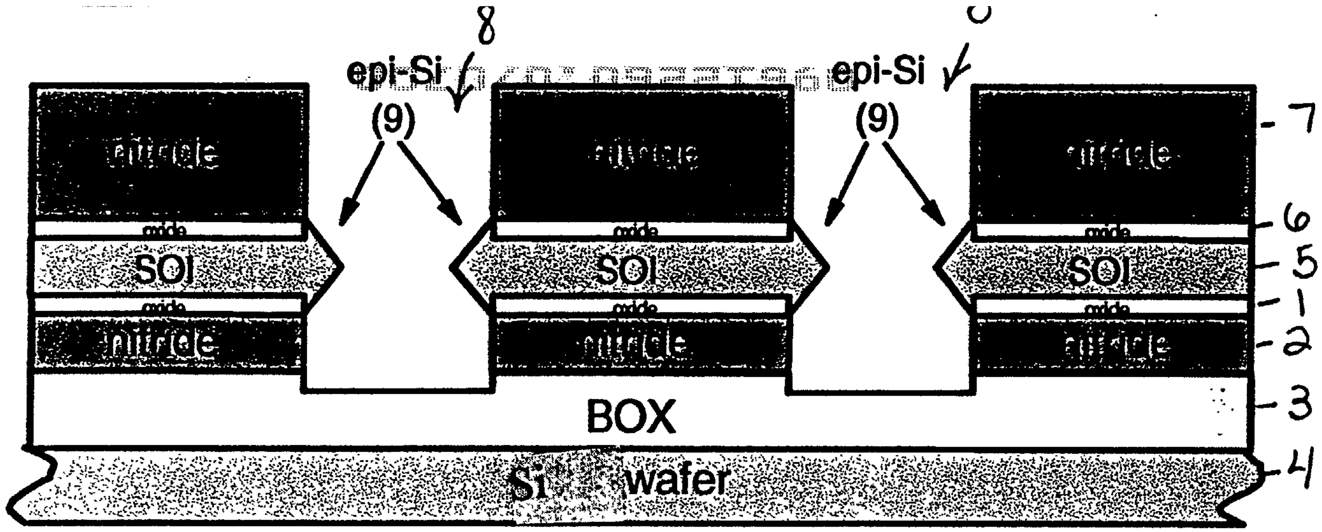


FIGURE 9

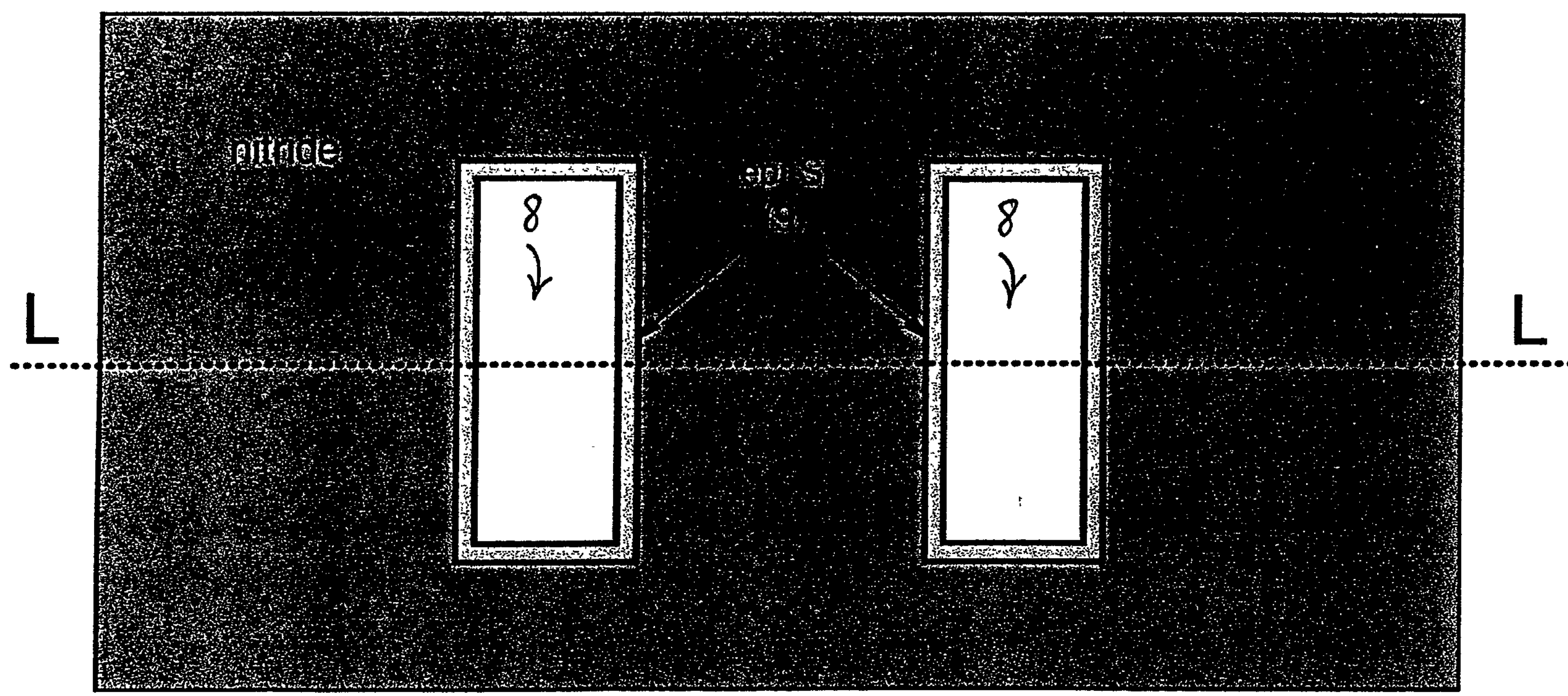


FIGURE 10

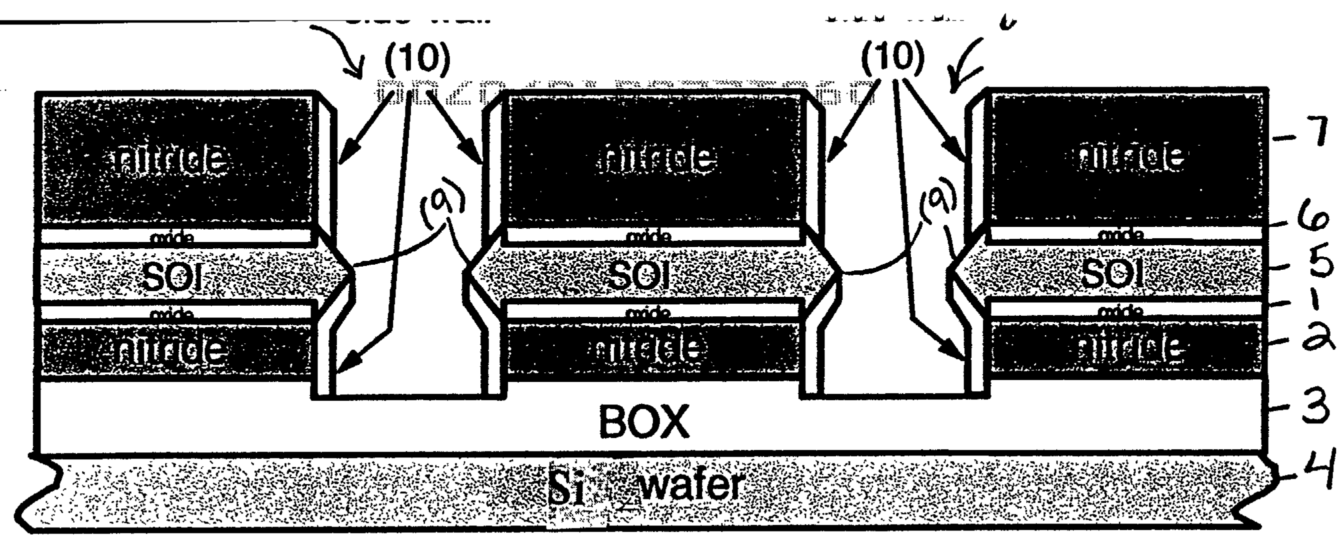


FIGURE 11

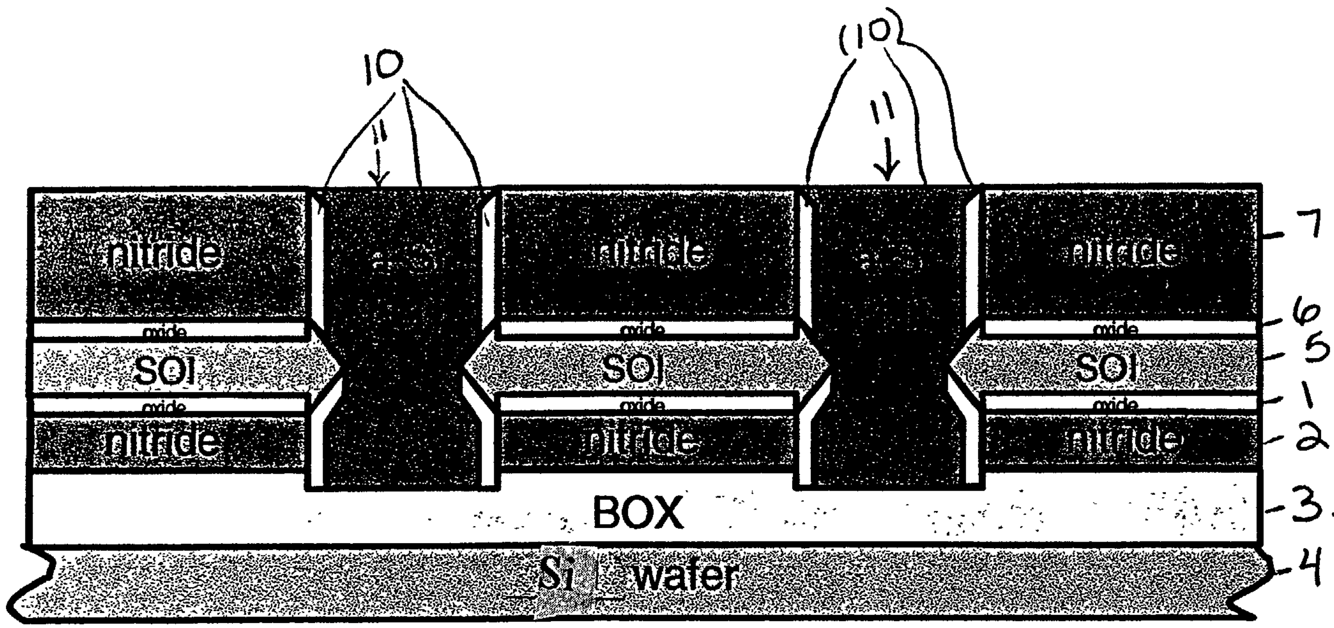


FIGURE 12

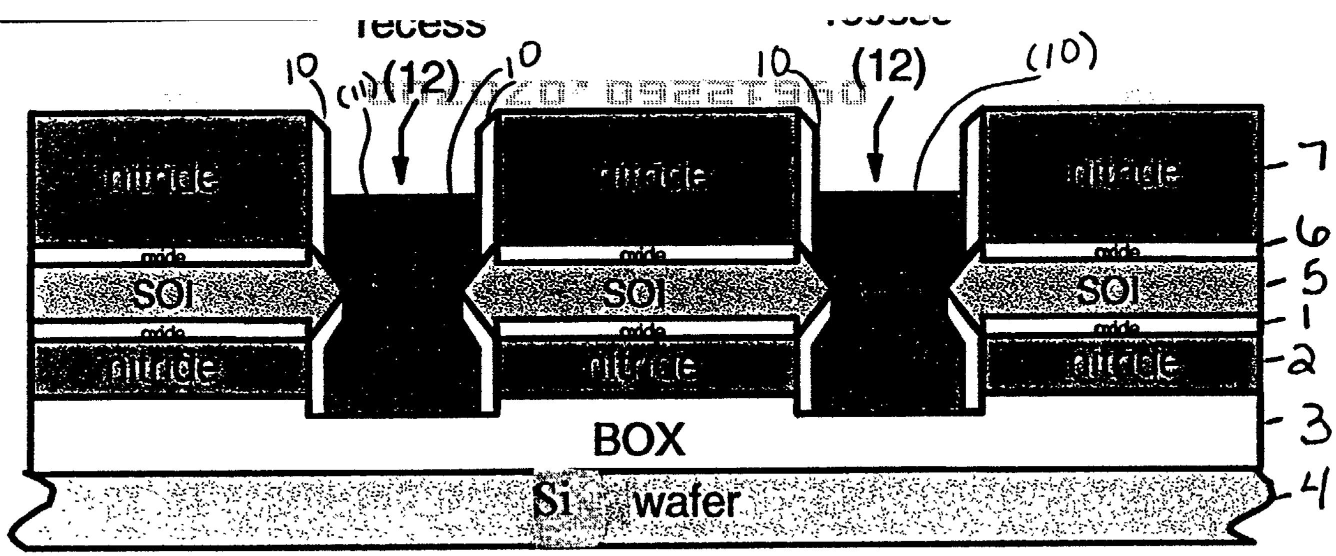


FIGURE 13

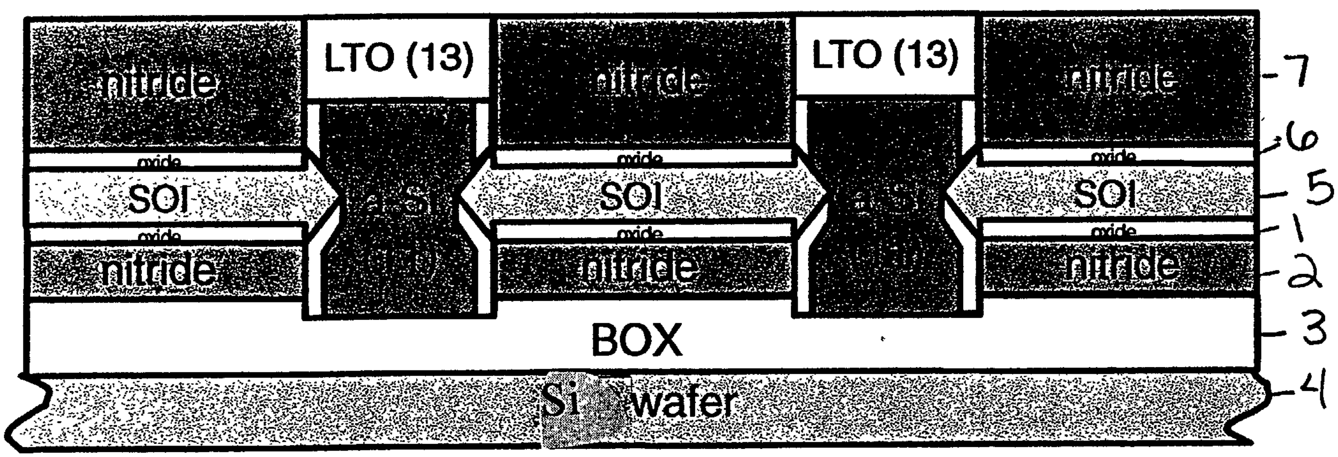


FIGURE 14

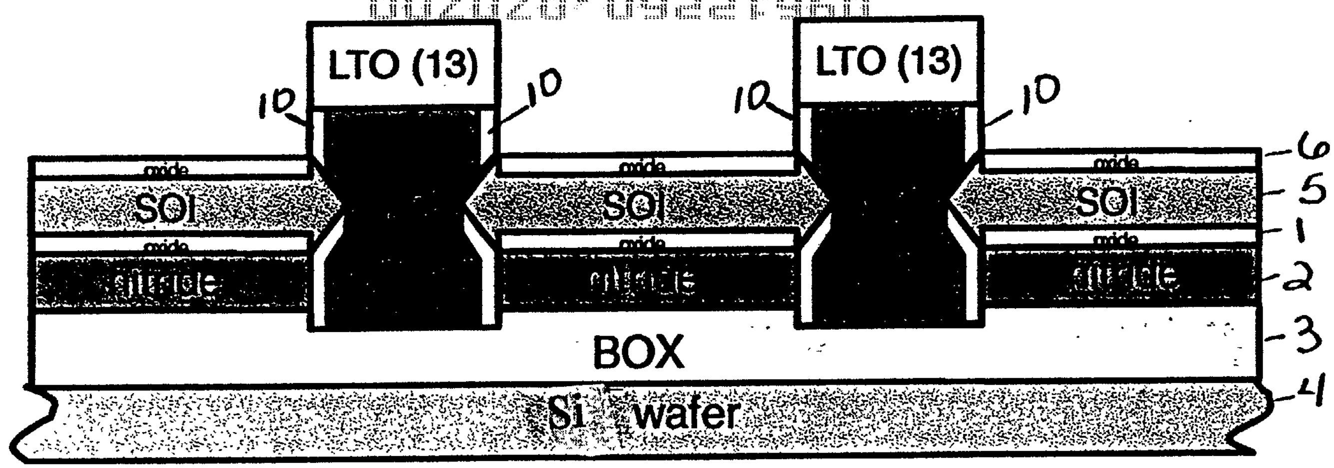


FIGURE 15

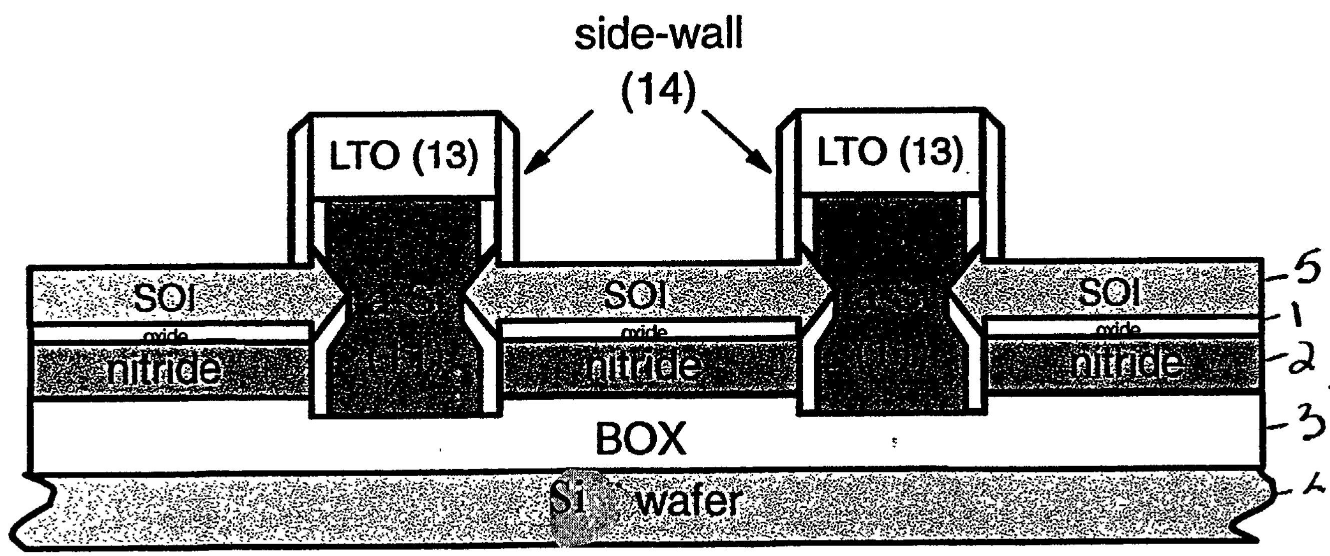
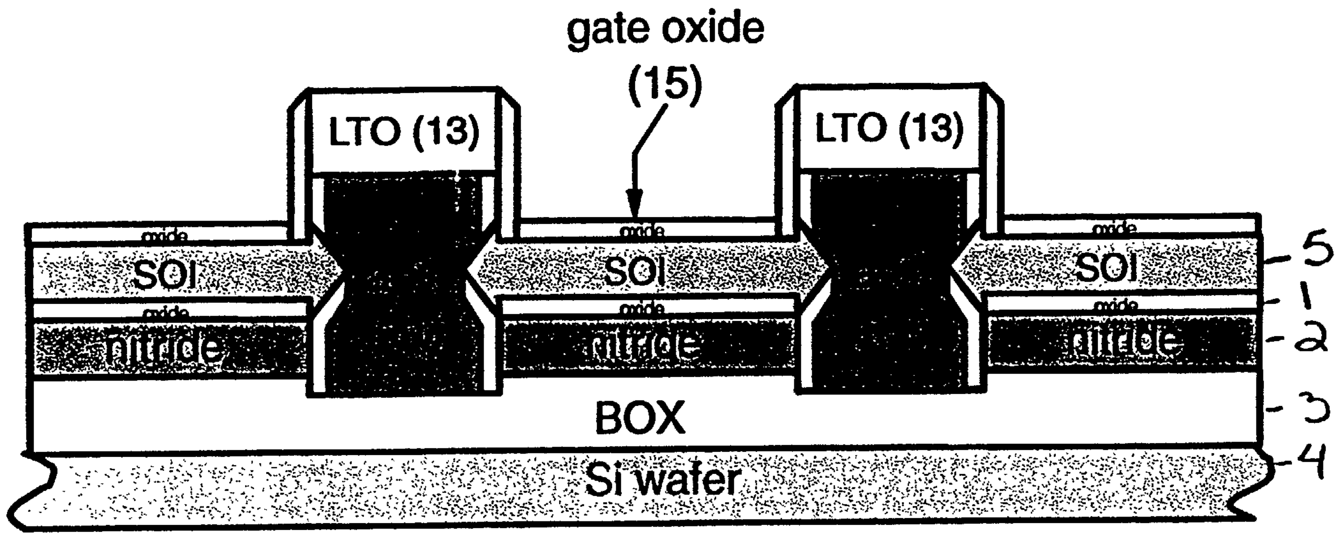


FIGURE 16



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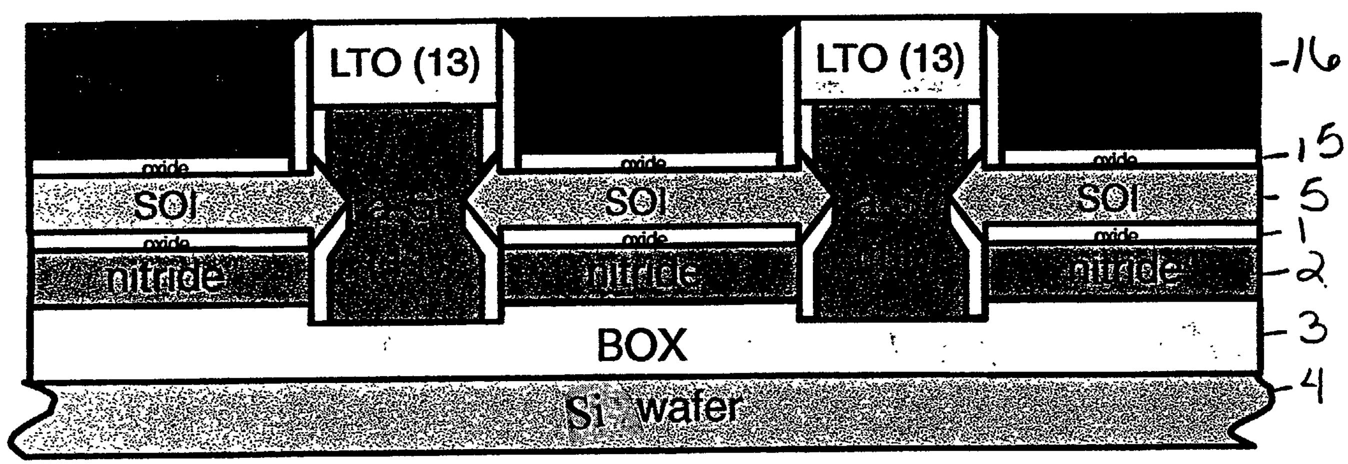
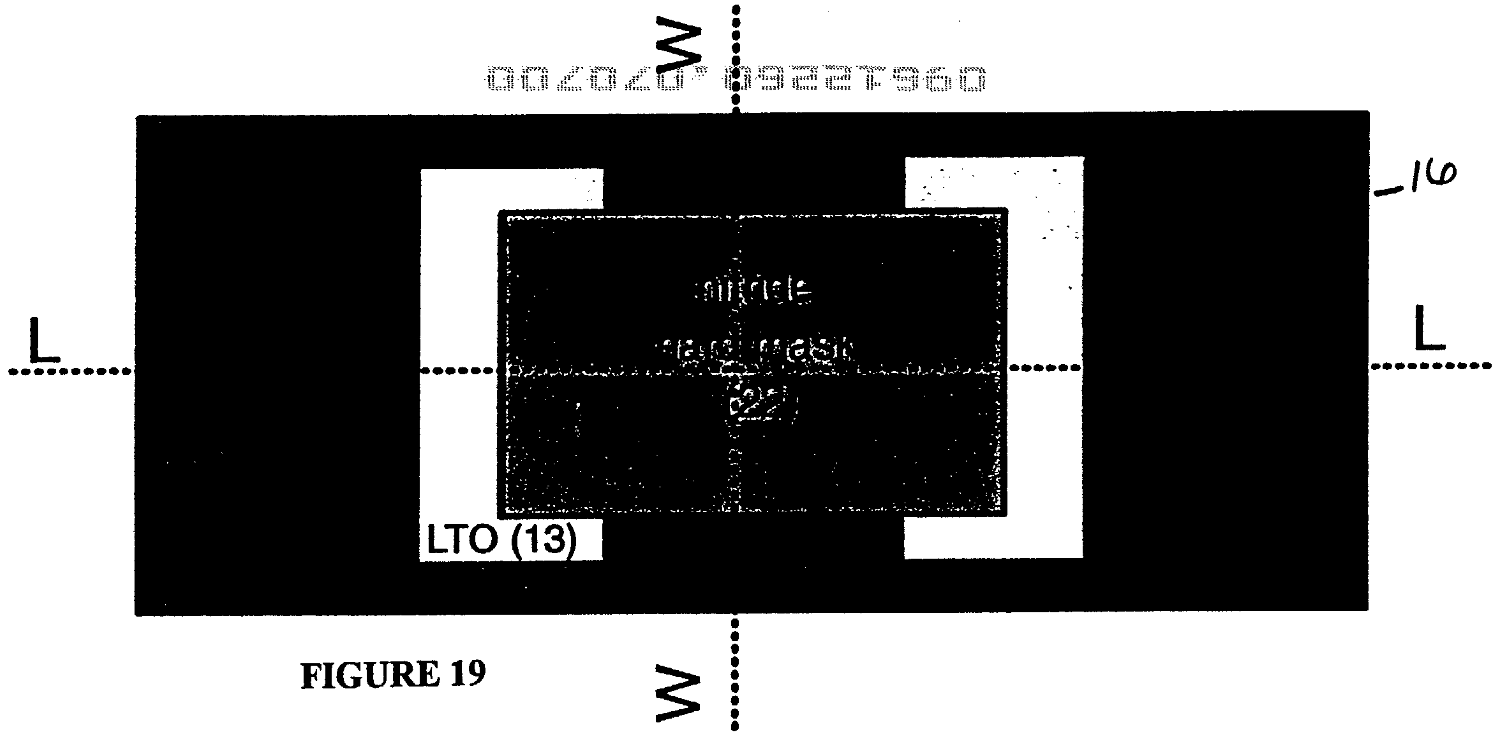


FIGURE 18



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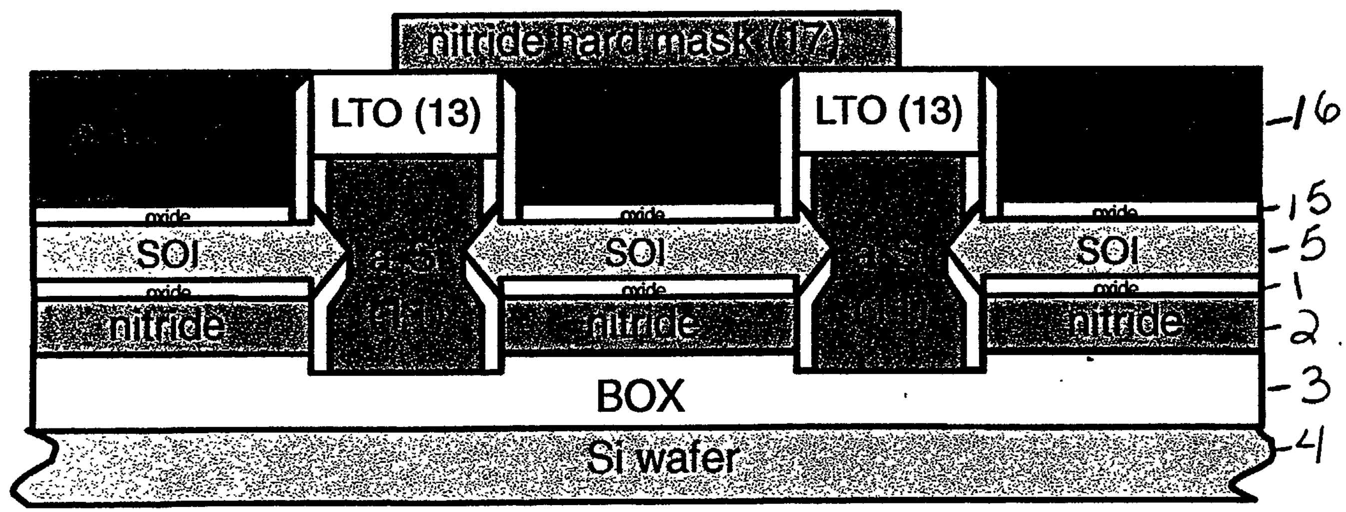
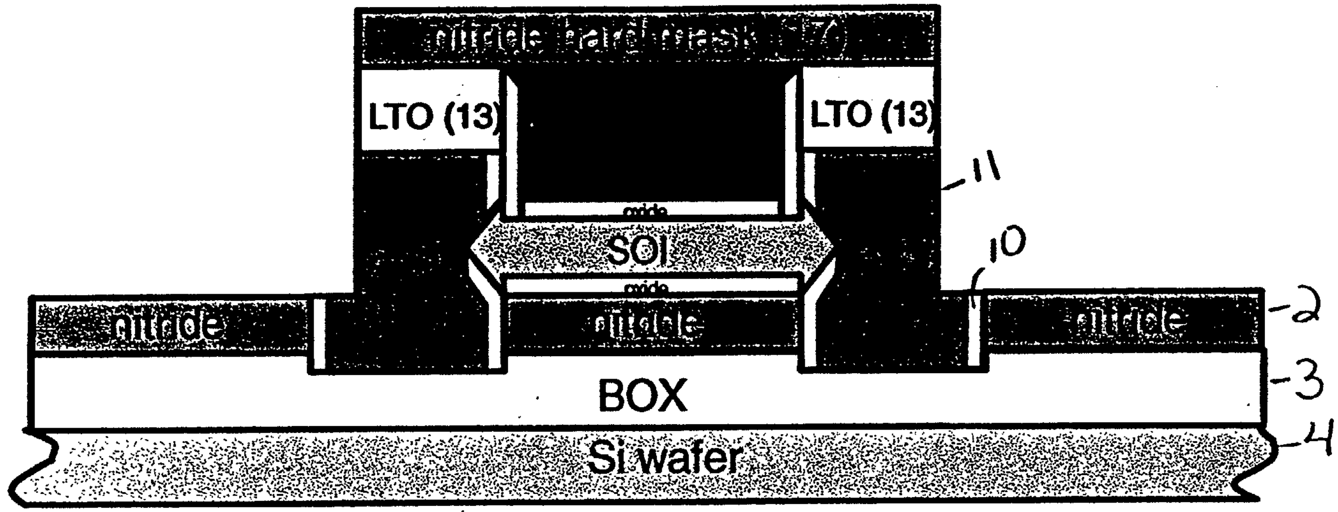


FIGURE 20



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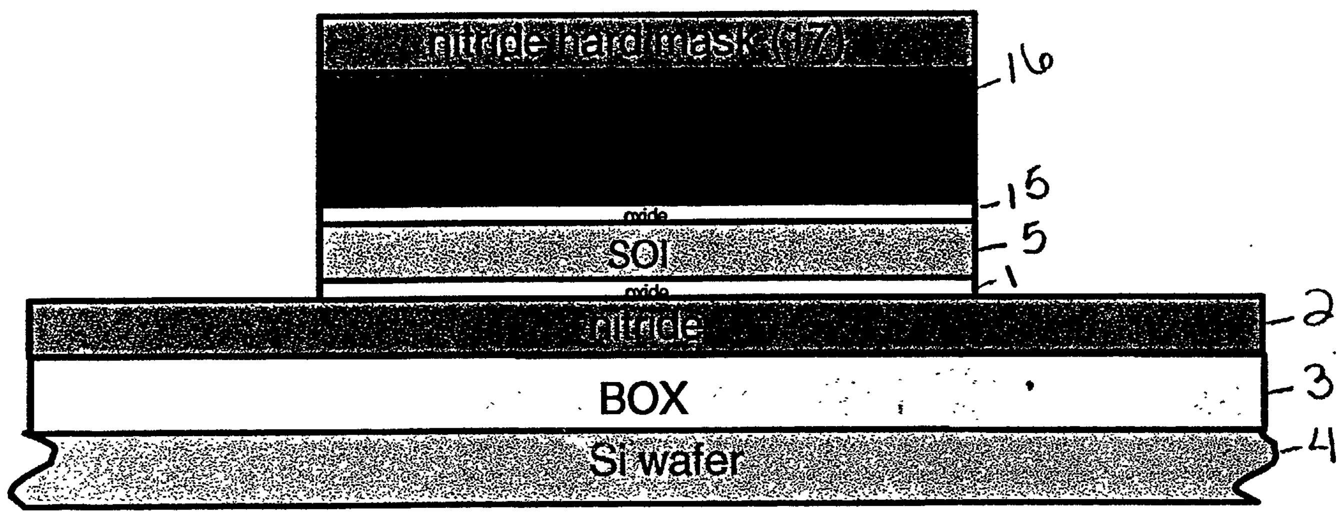

FIGURE 22

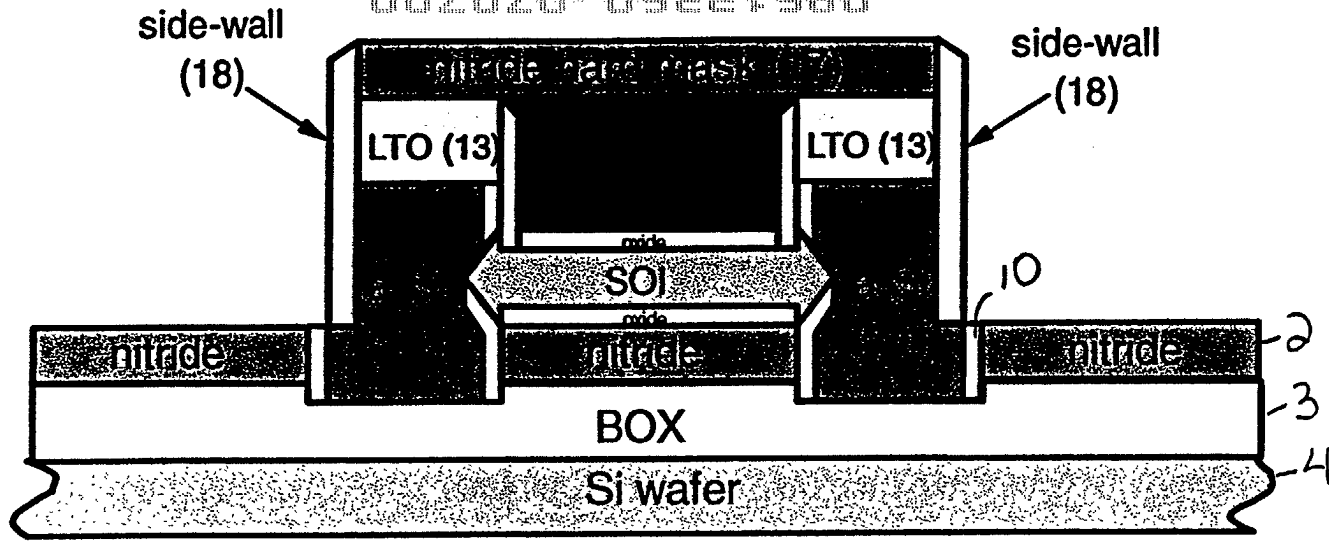

FIGURE 23

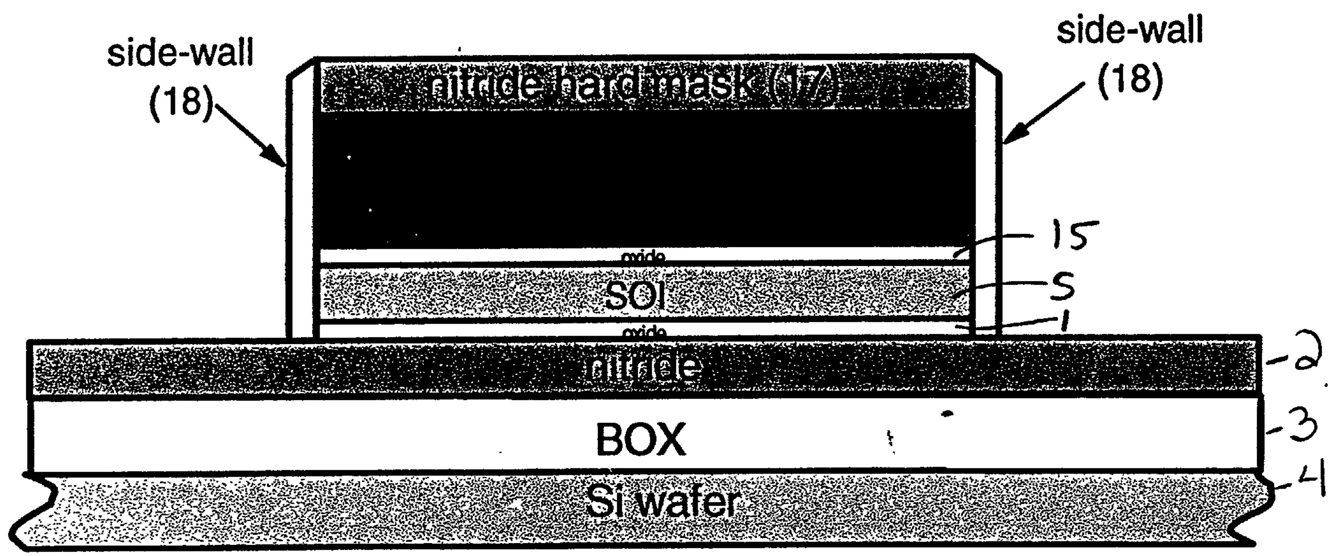

FIGURE 24

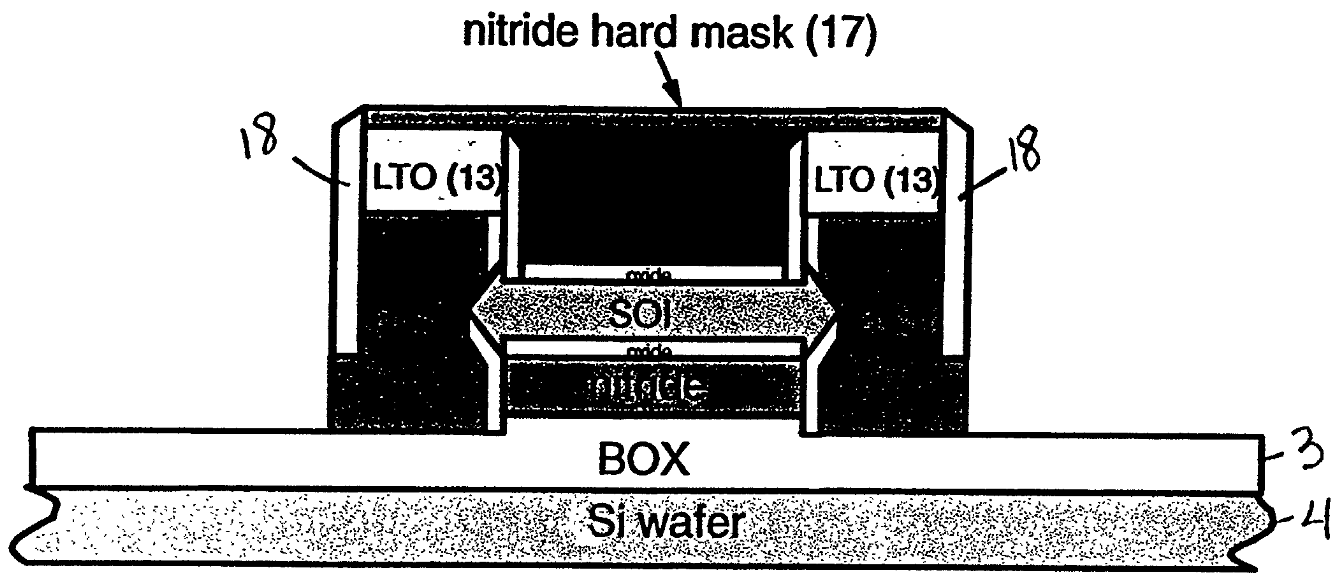

FIGURE 25

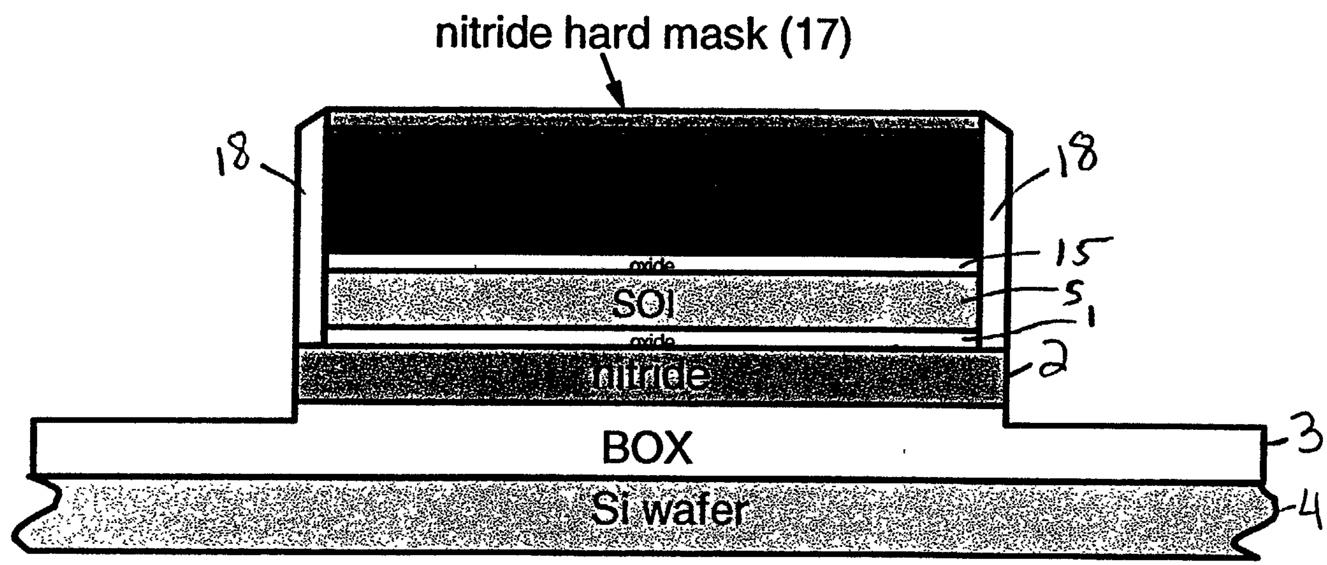

FIGURE 26

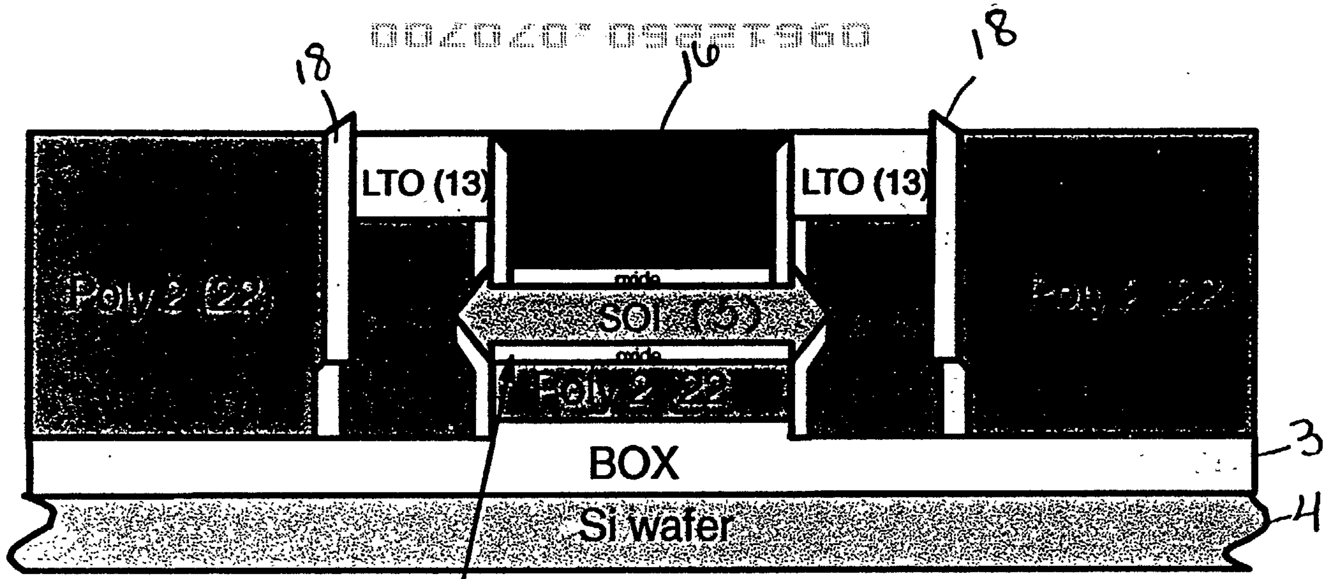

FIGURE 31

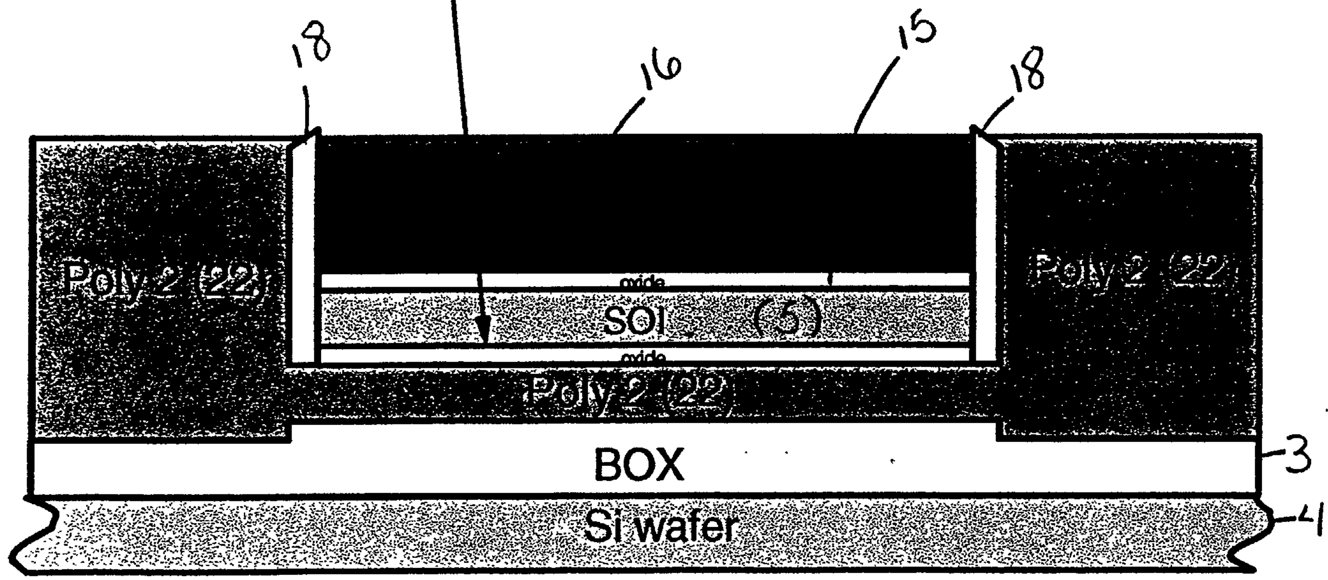

FIGURE 32

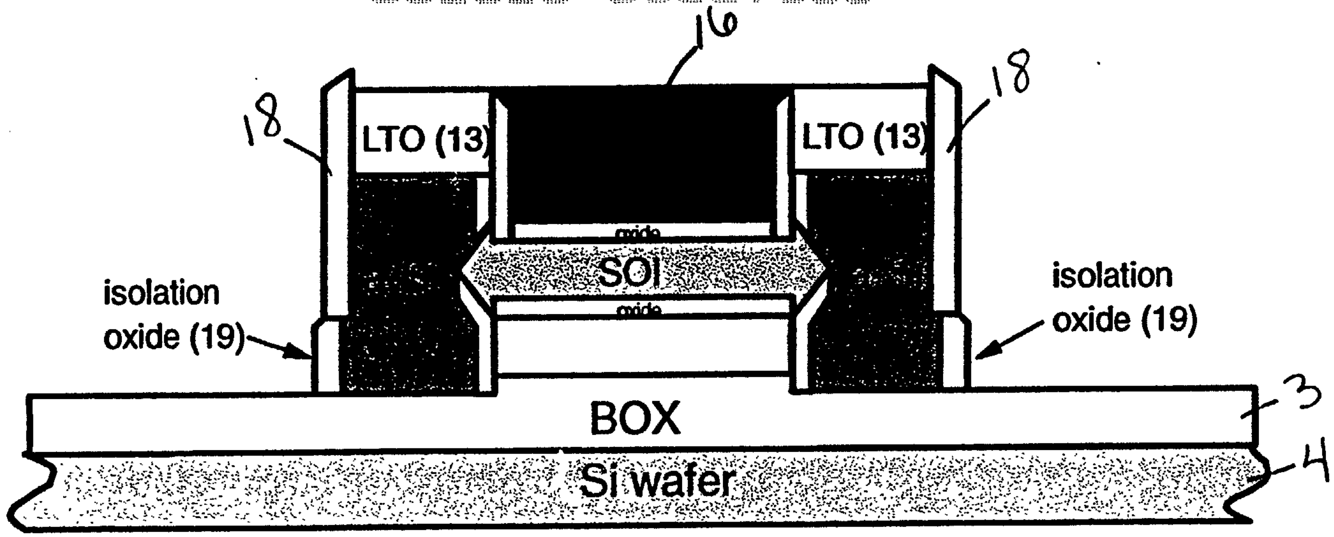

FIGURE 29

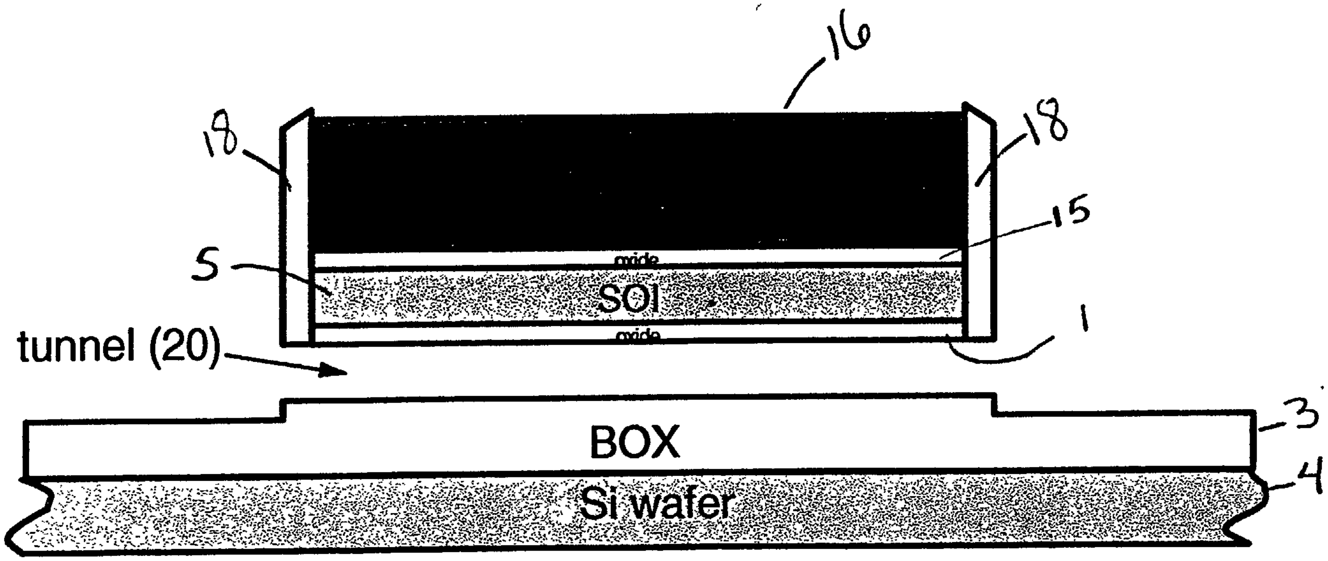

FIGURE 30

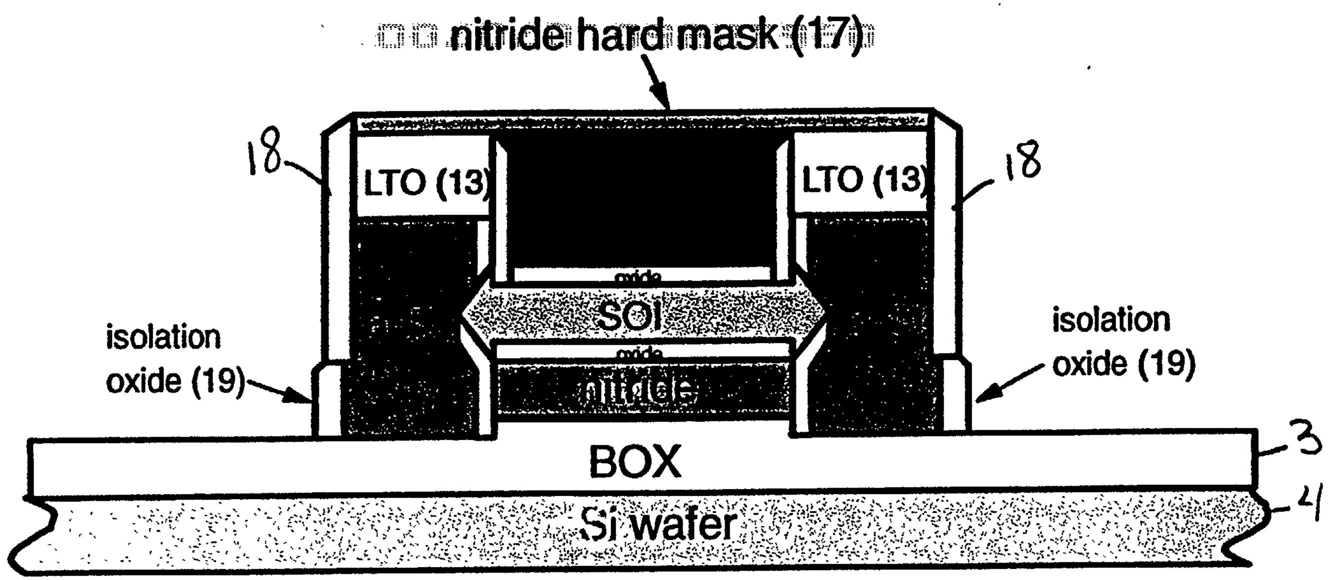

FIGURE 27

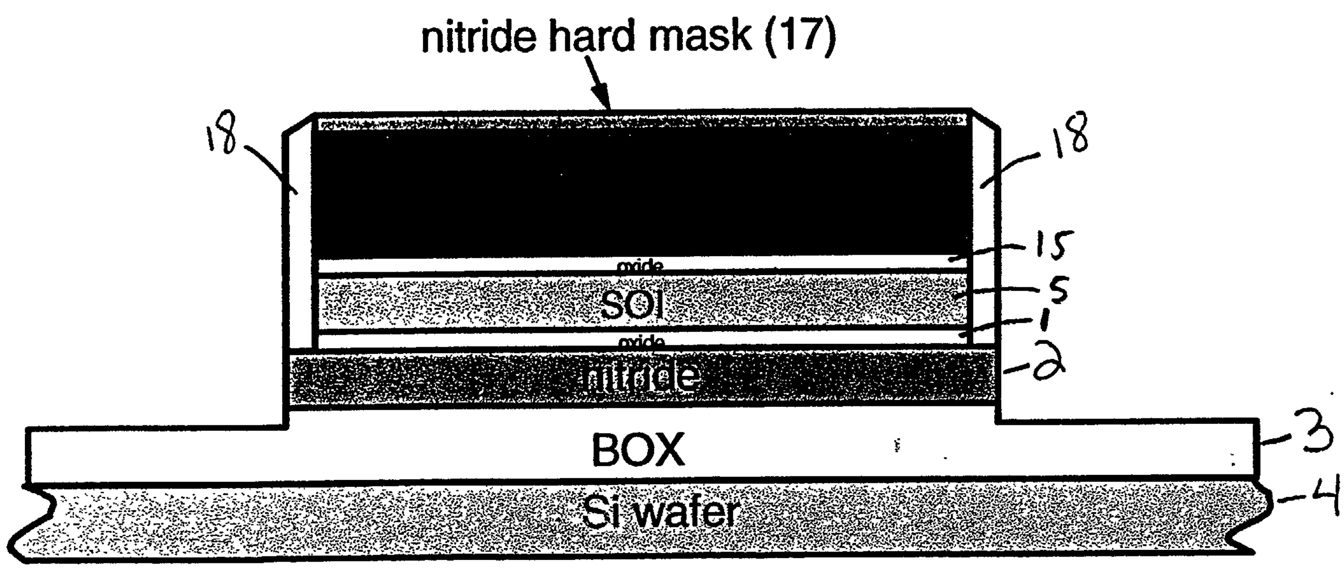

FIGURE 28

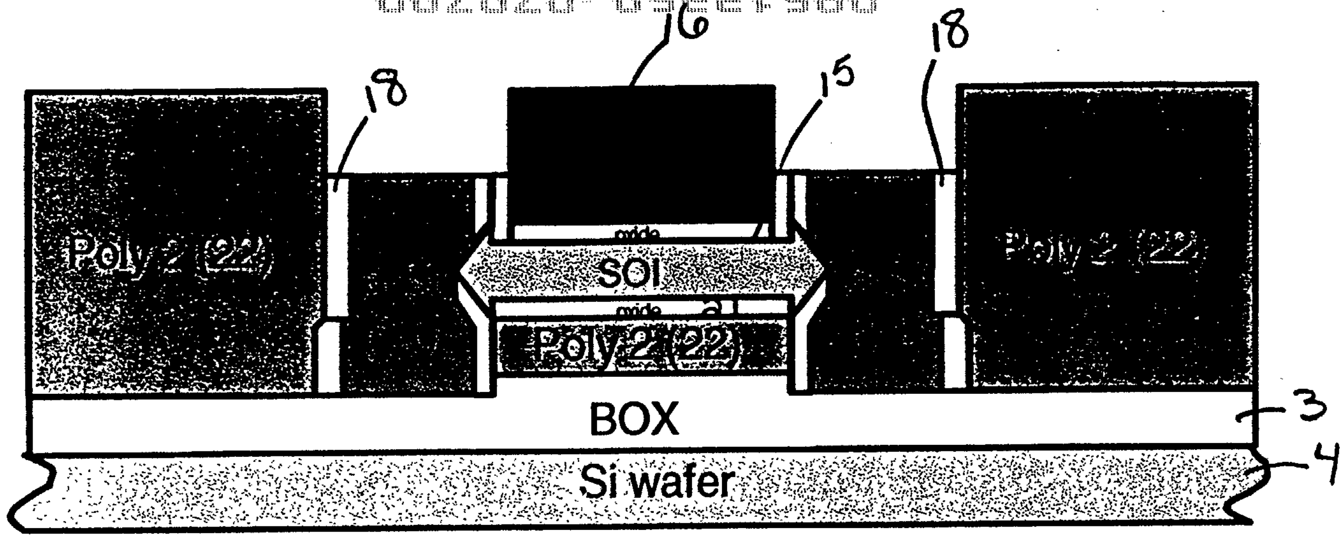

FIGURE 33

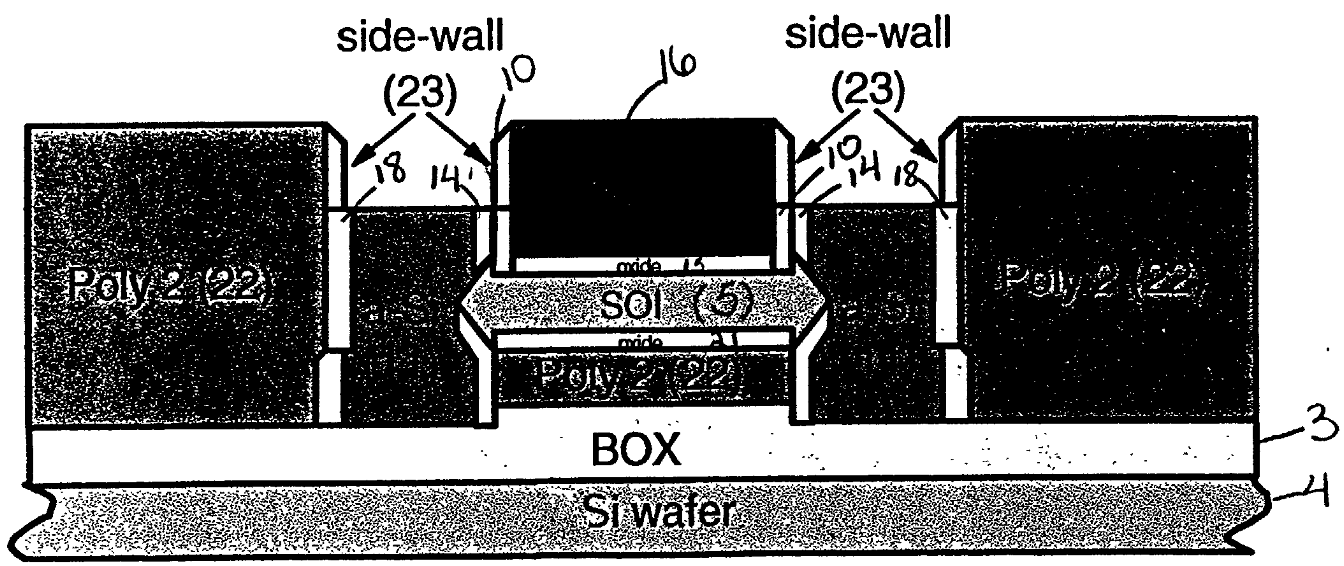

FIGURE 34

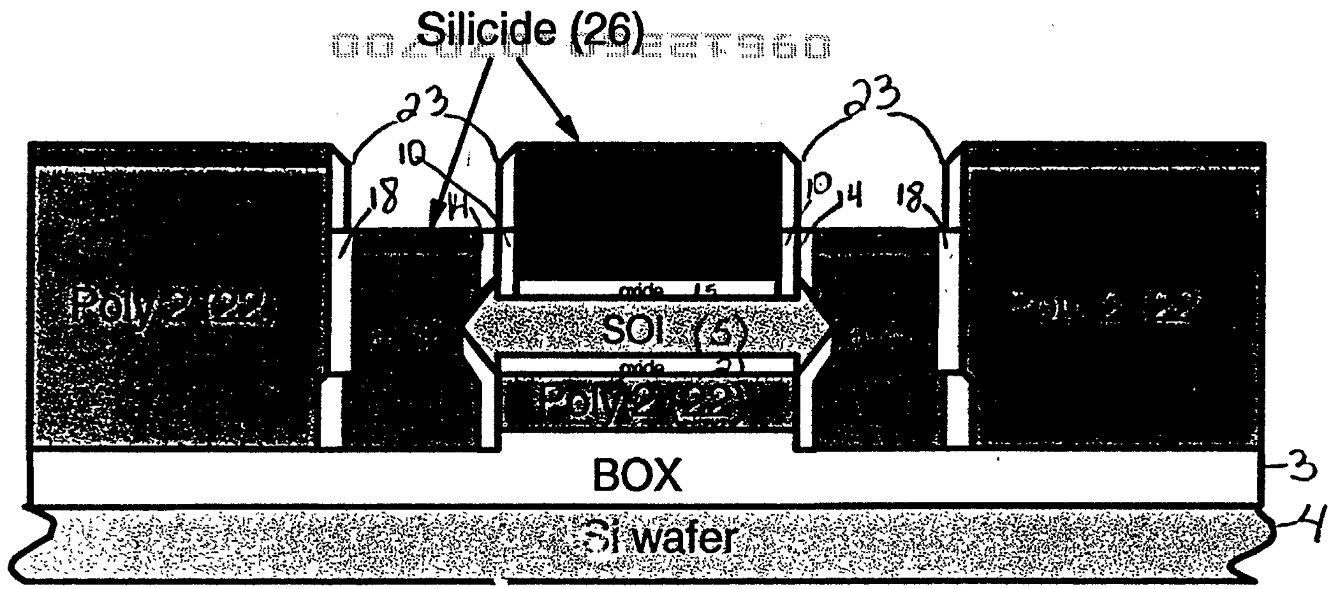

FIGURE 37

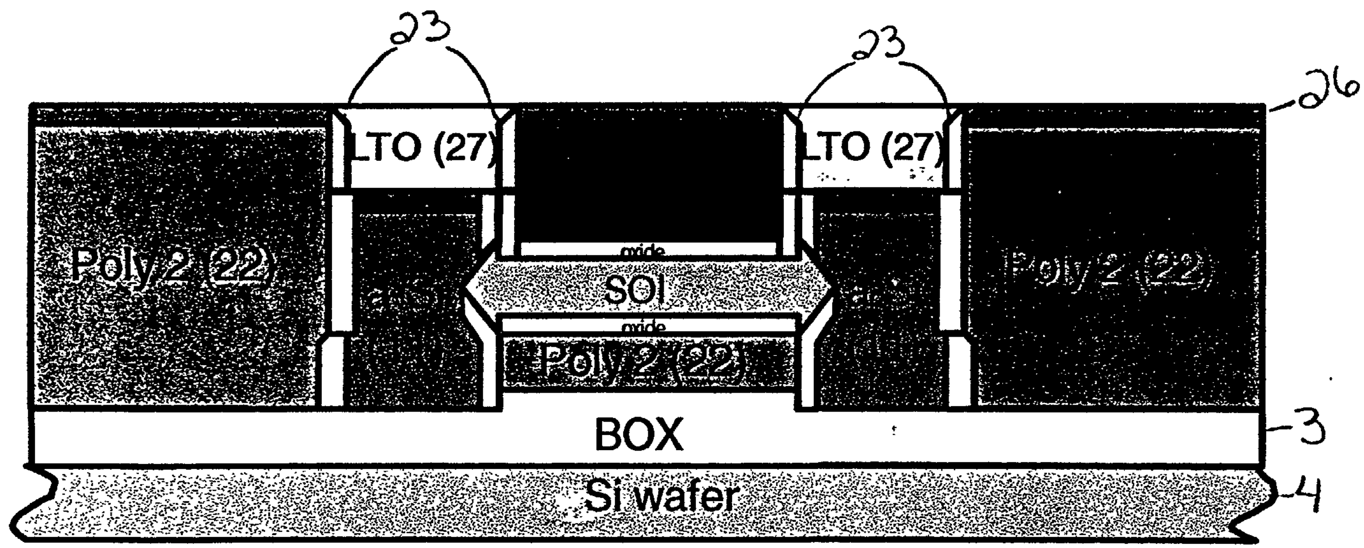

FIGURE 38

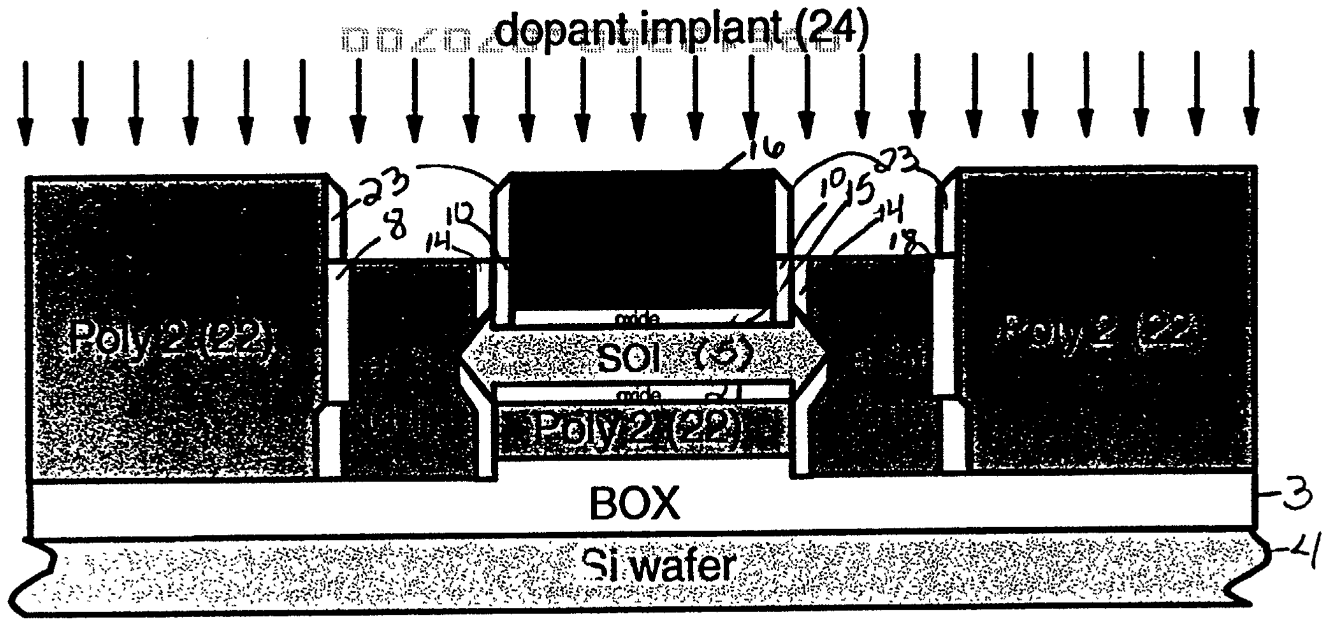

FIGURE 35

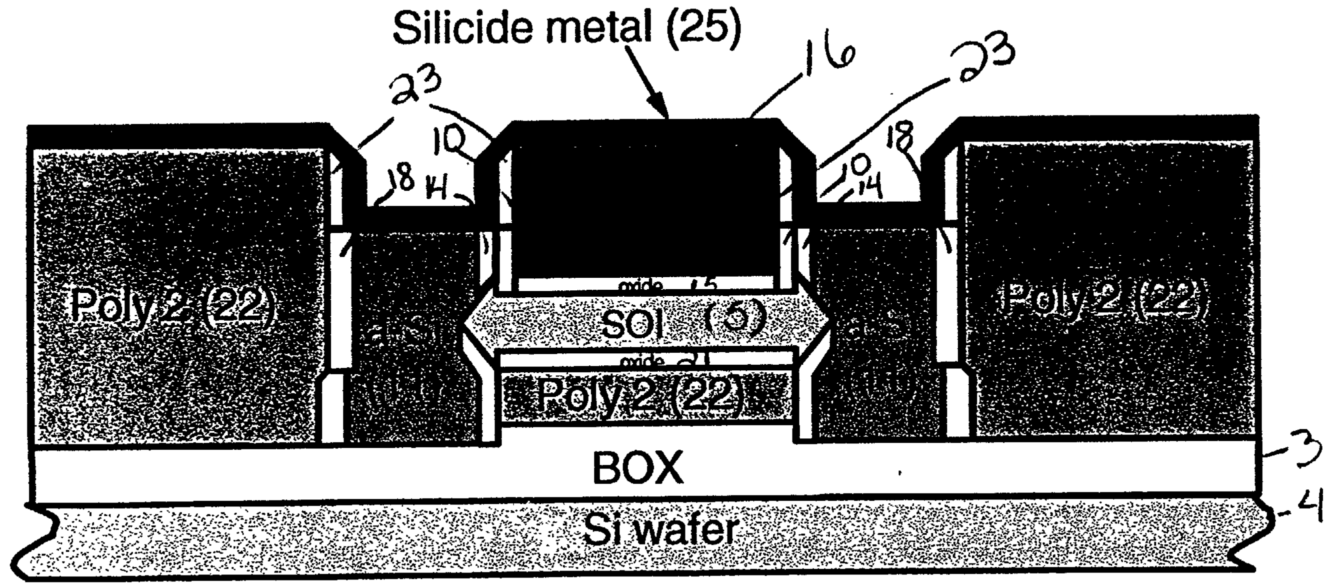

FIGURE 36

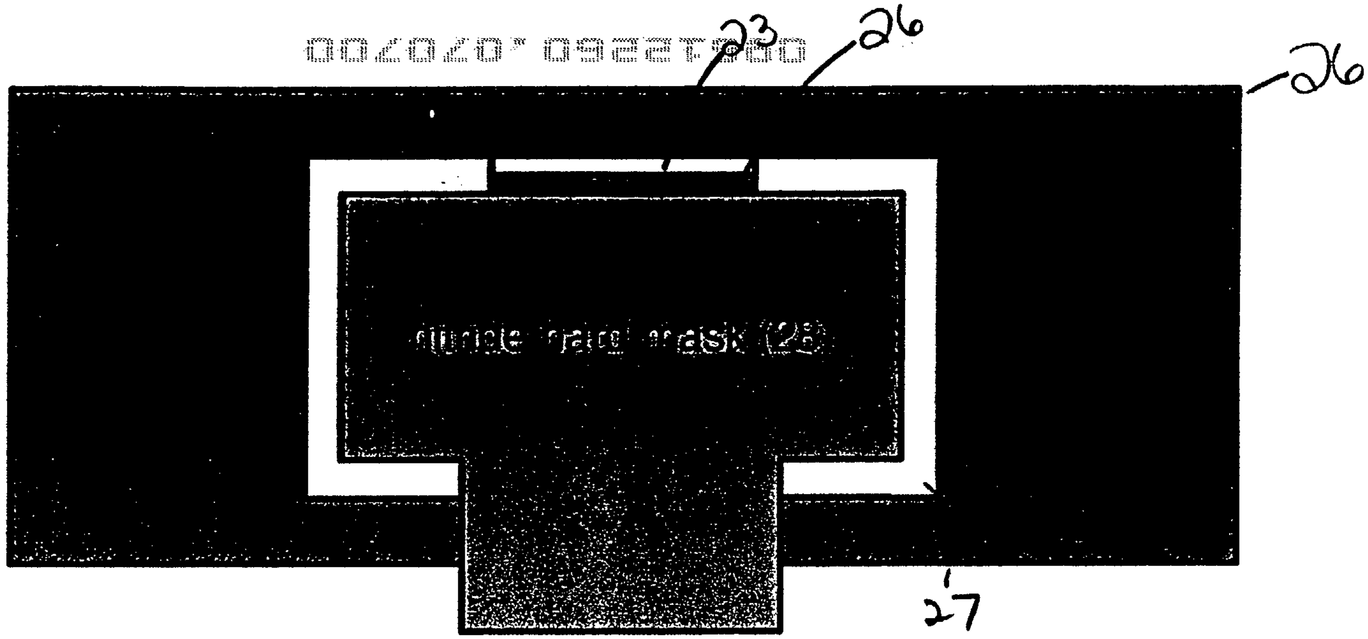

FIGURE 39

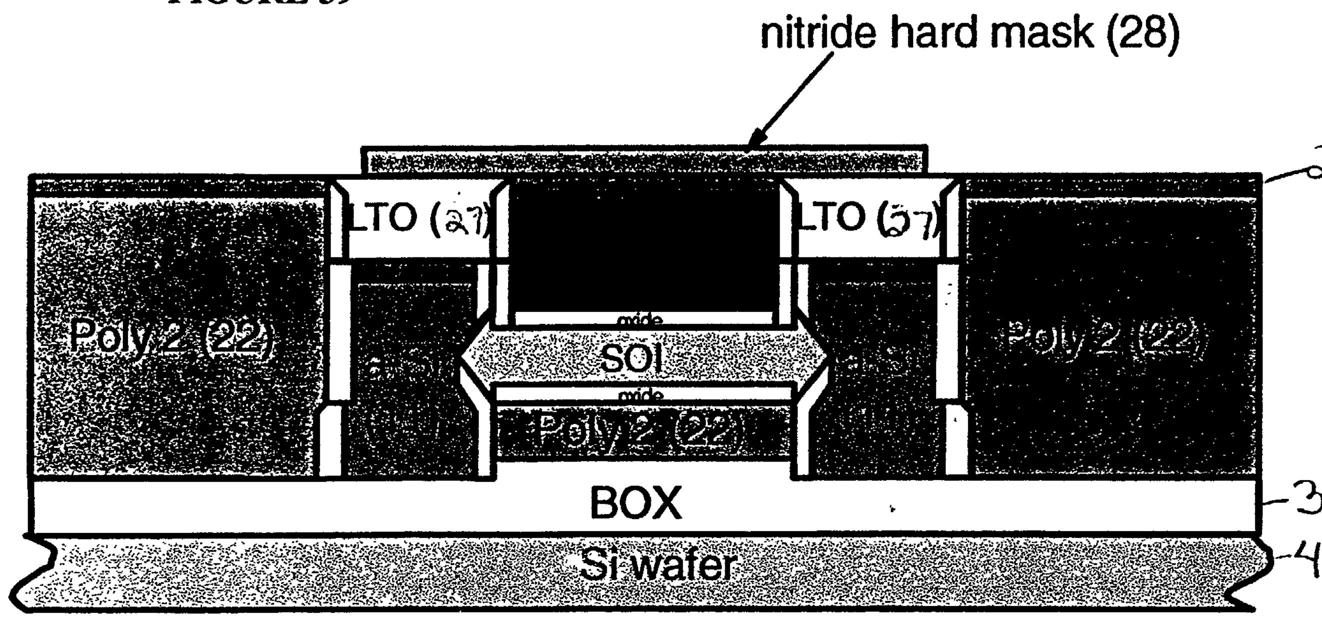

FIGURE 40

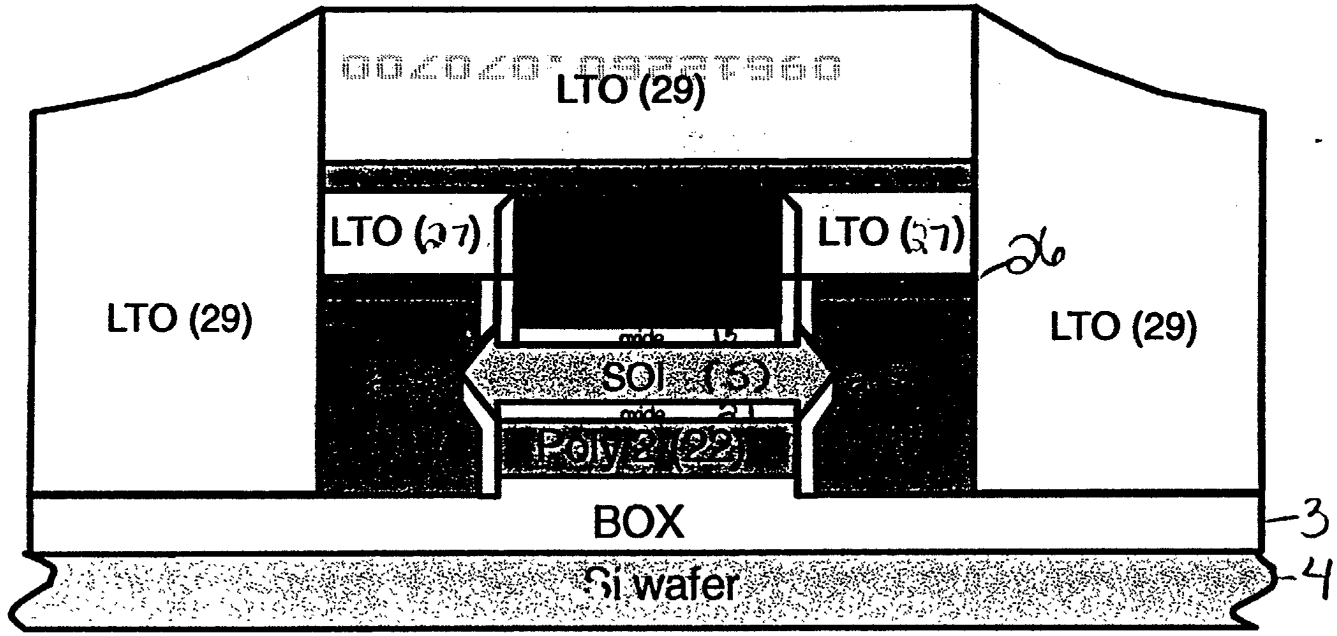

FIGURE 41

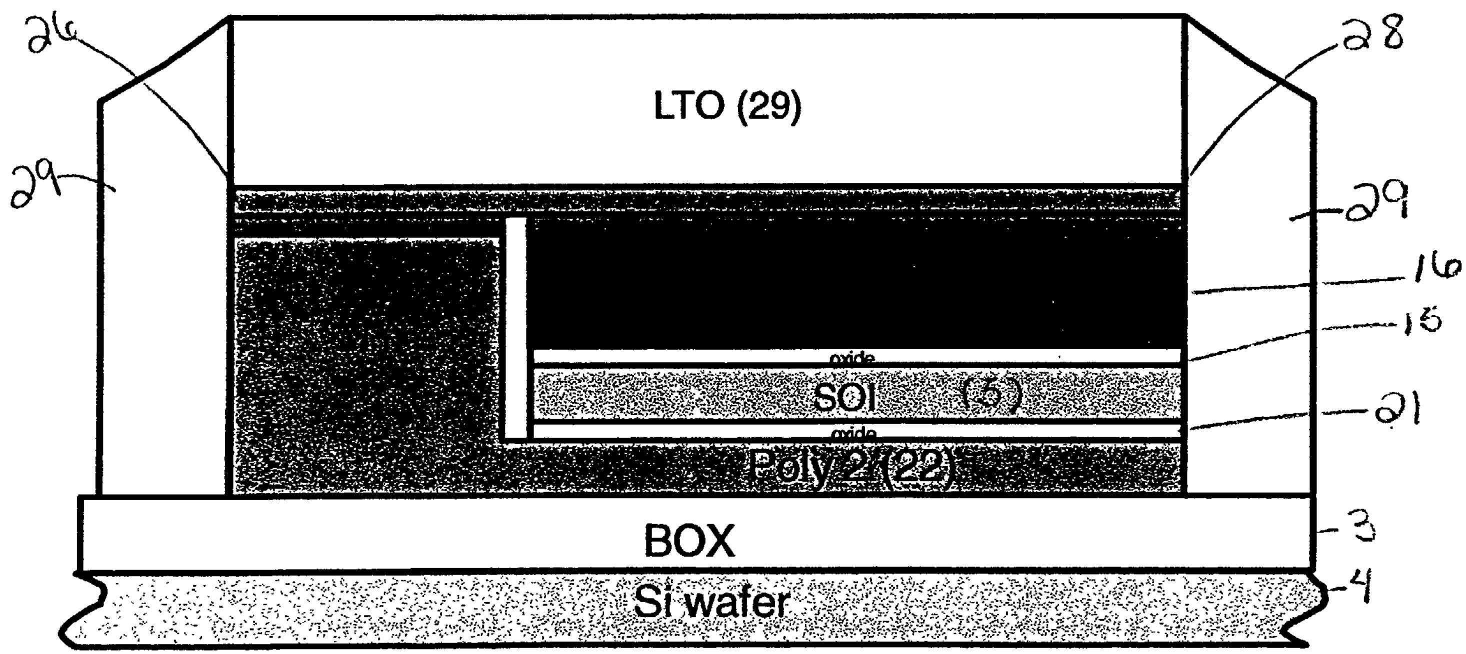

FIGURE 42

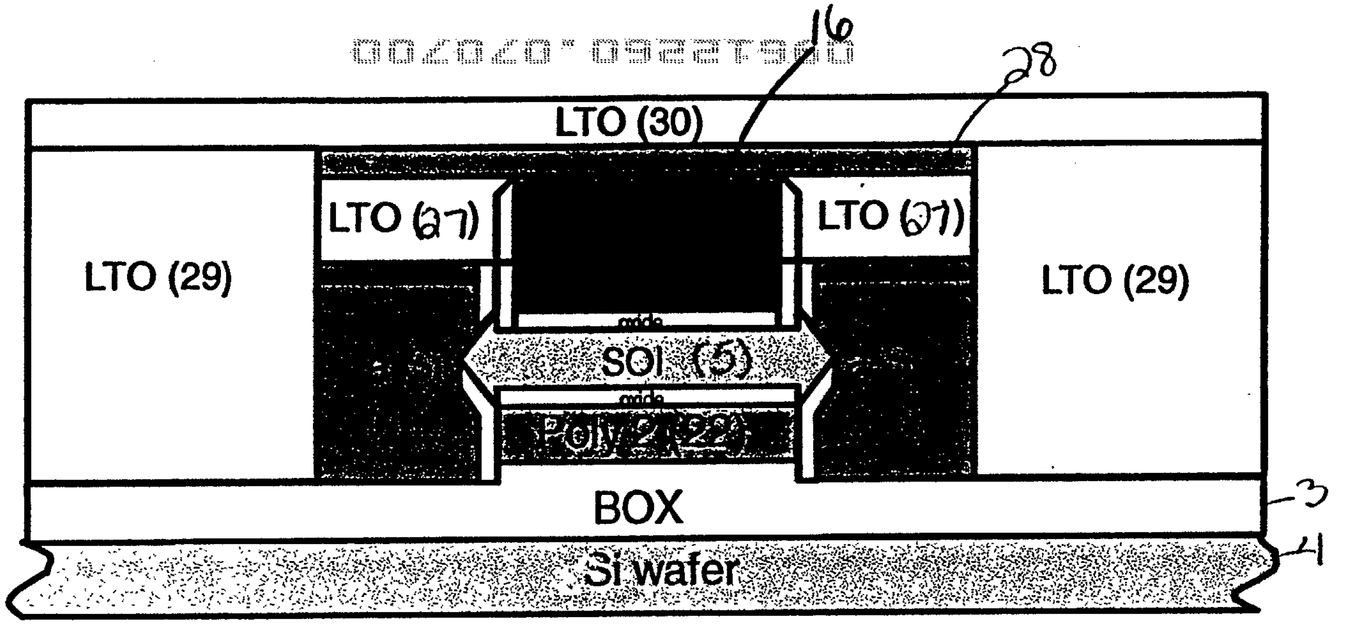

FIGURE 43

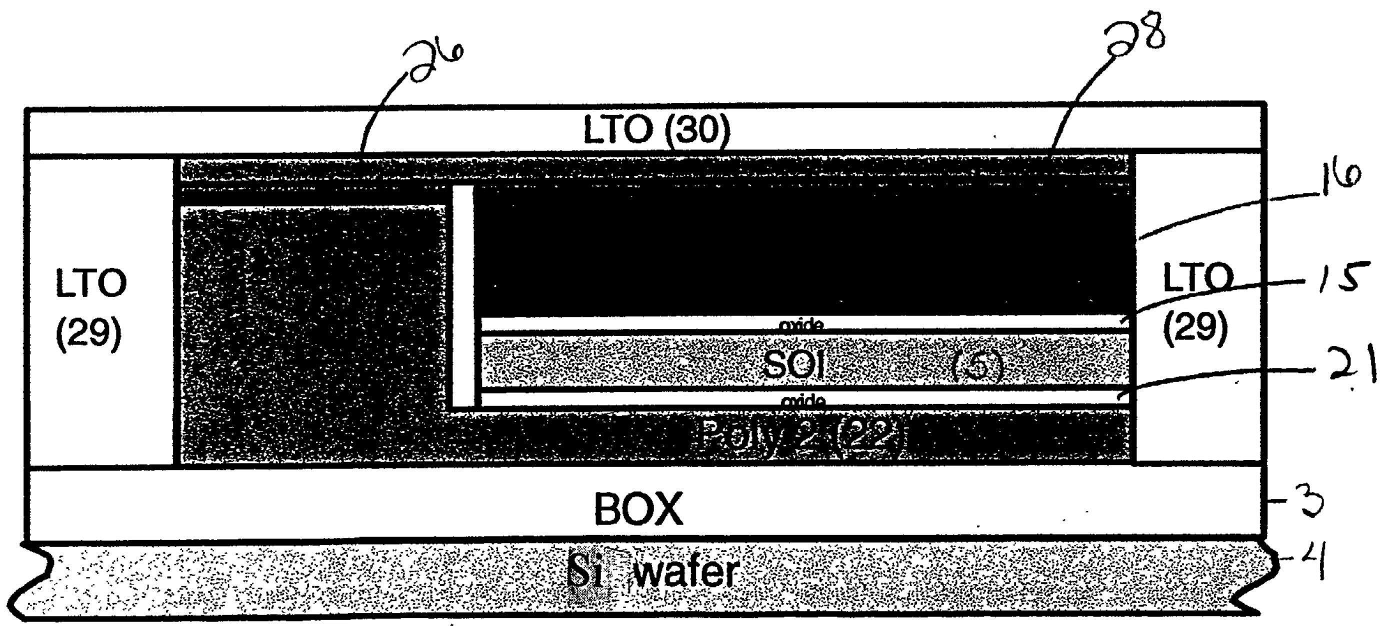

FIGURE 44

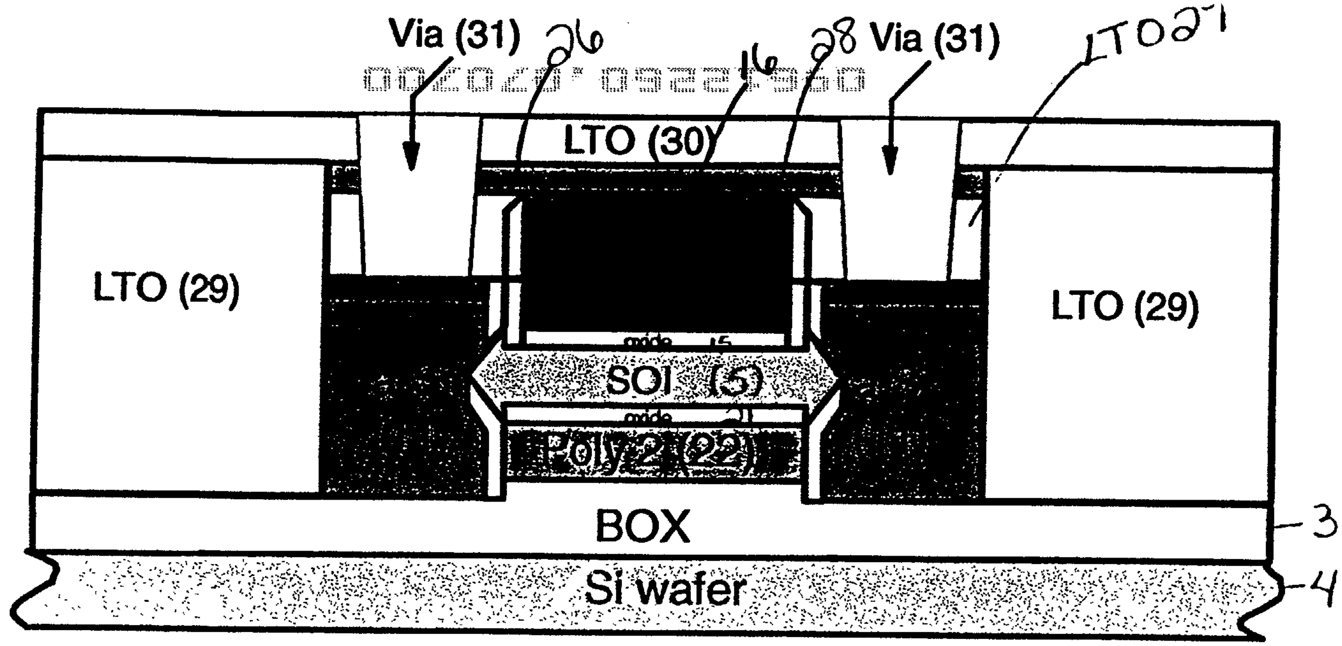

FIGURE 45

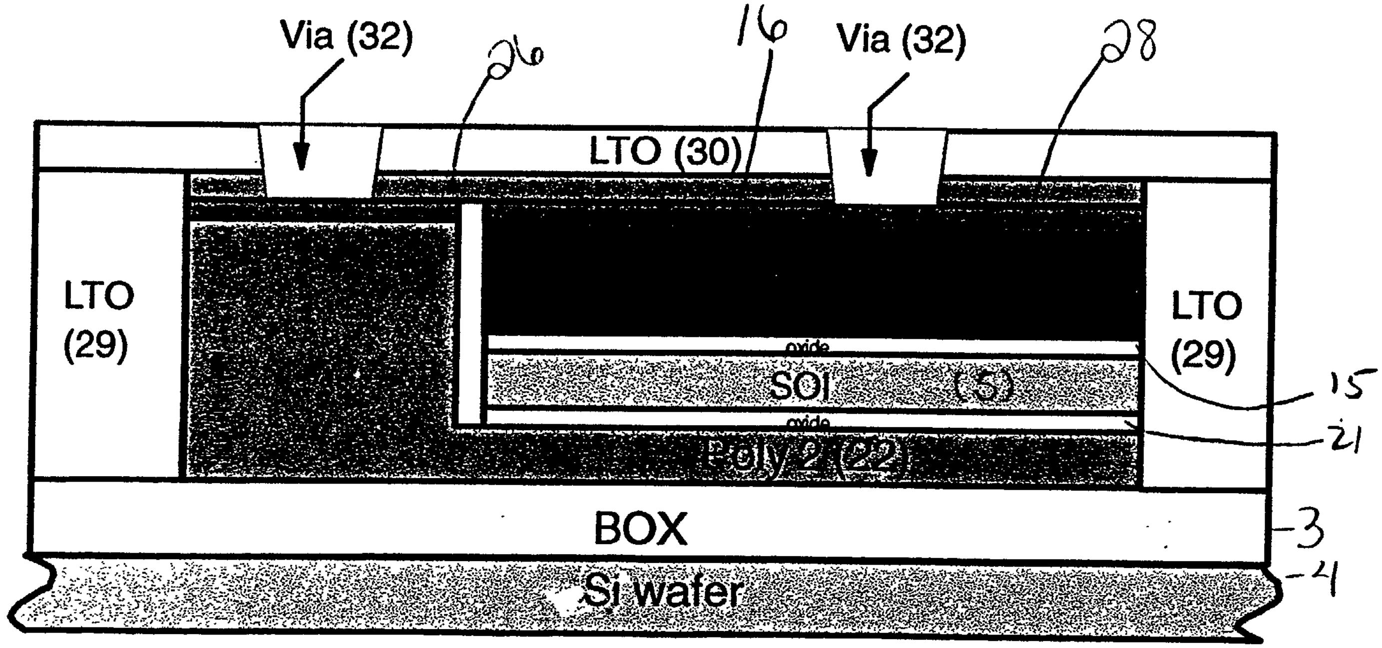

FIGURE 46

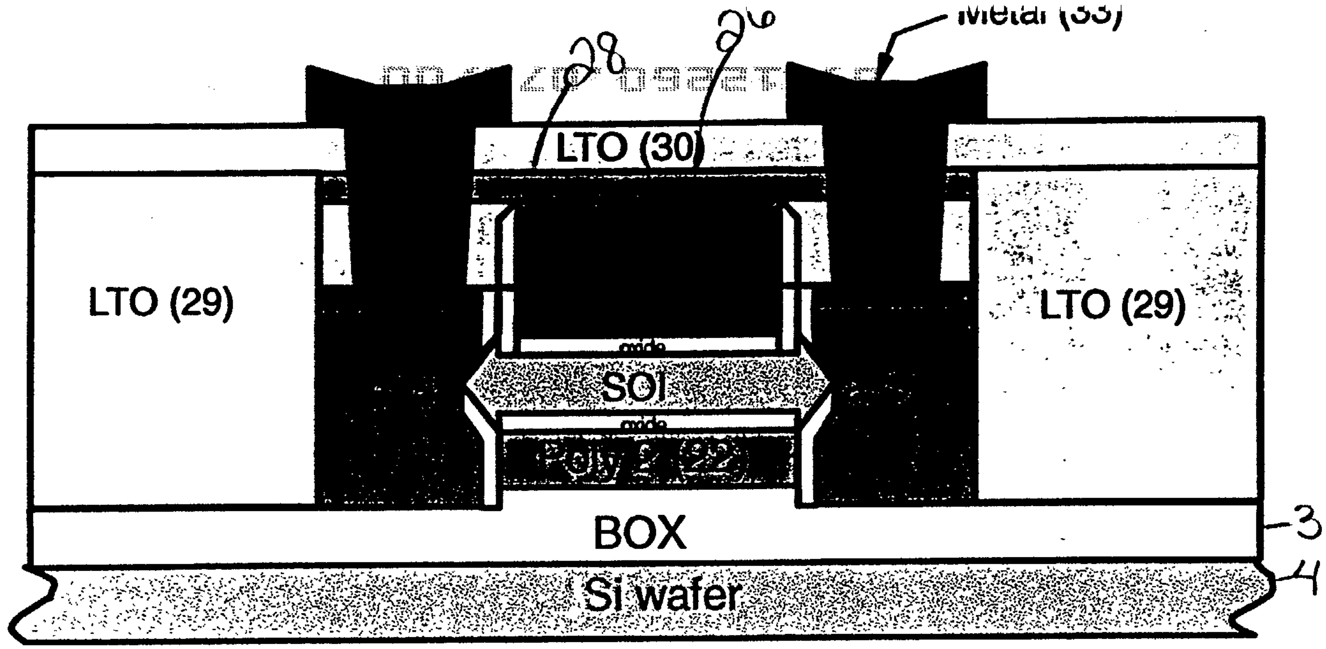

FIGURE 47

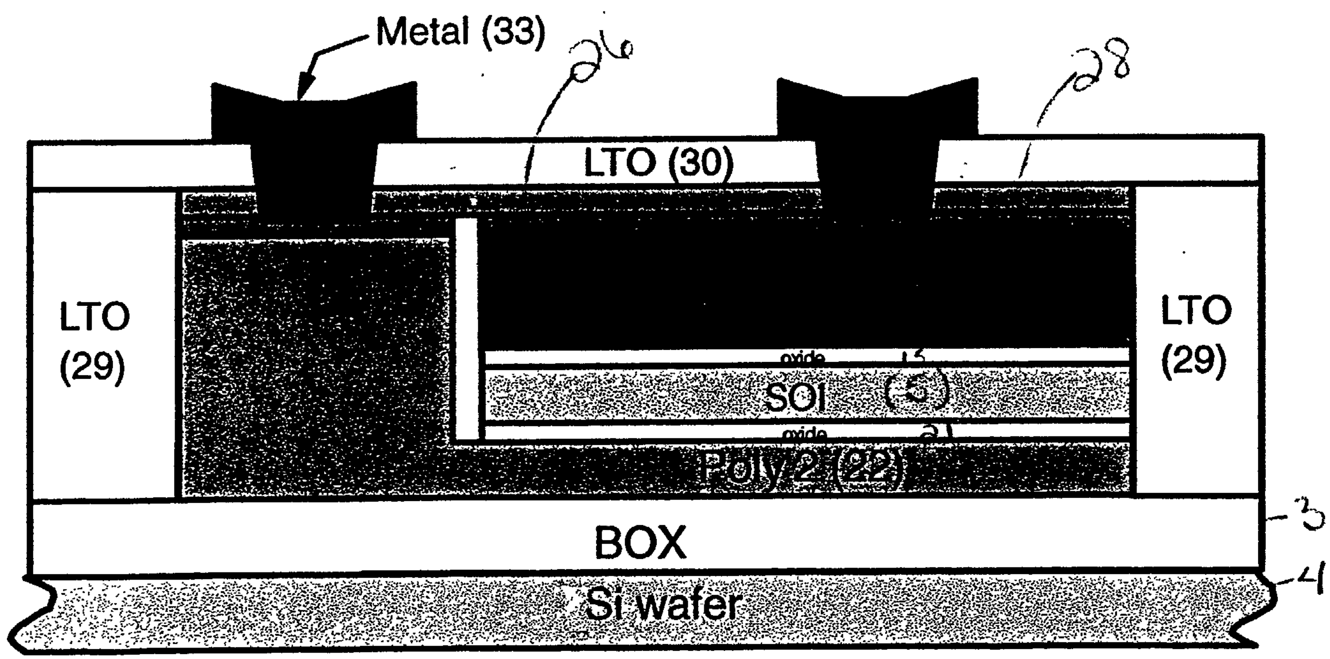

FIGURE 48

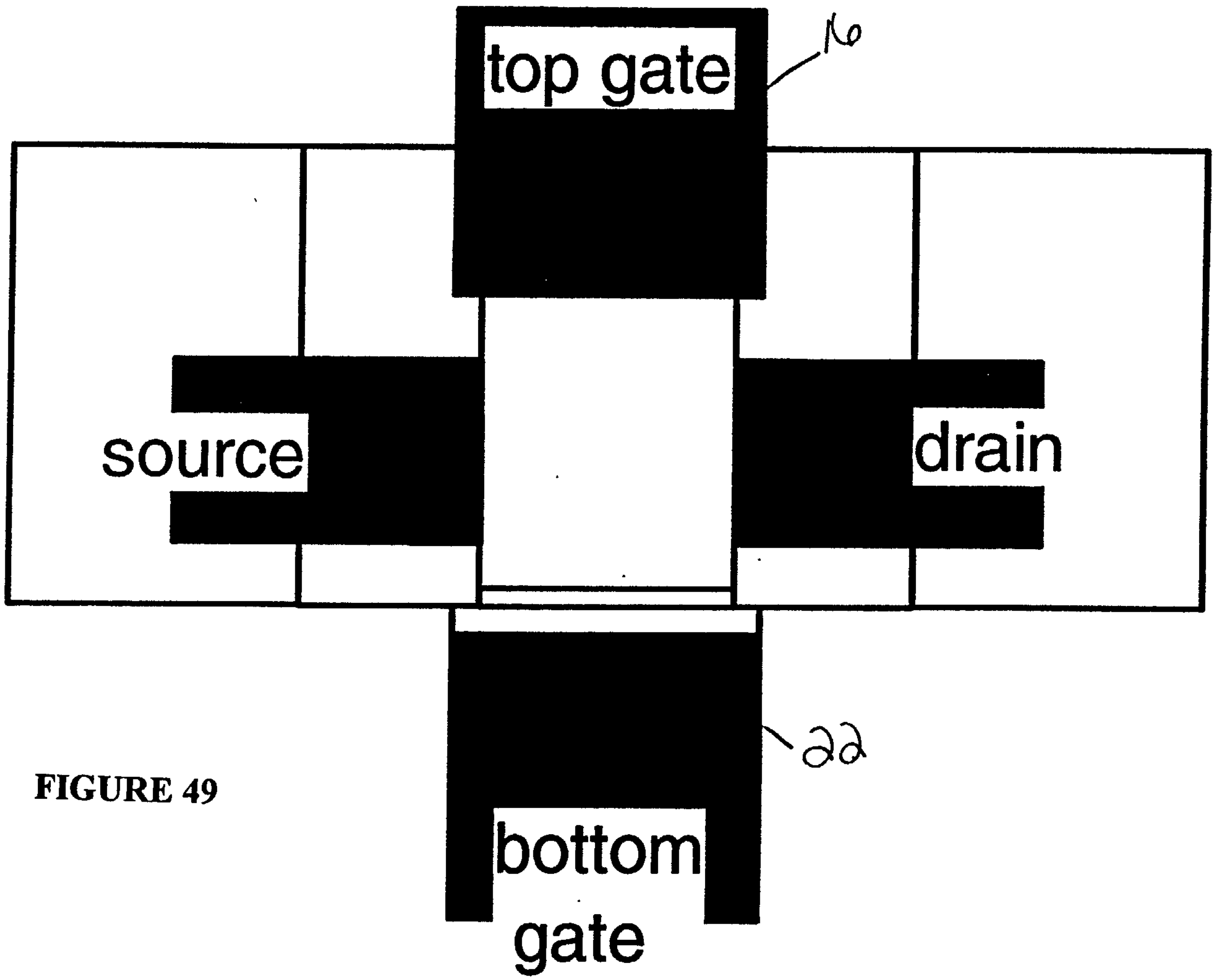

FIGURE 49

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SYSTEM-ALIGNED GATE MOSFET WITH SEPARATE GATES

the specification of which:
(check one)

☒ is attached hereto.
☐ was filed on ________________, as Application Serial No. ________________ and was amended on __________.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Day/Month/Year	Priority Claimed

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.	Filing Date	Status
00/__________	May 15, 2000	Pending

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Tide 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: We hereby appoint Manny Schecter, Registration No.31,722, Lauren Bruzzone, Registration No. 35,082, Christopher A. Hughes, Registration No. 26,914, Edward A. Pennington, Registration No. 32,588, John E. Hoel, Registration No. 26,279, Joseph C. Redmond, Jr., Registration No. 18,753, Douglas W. Cameron, Registration No. 31,596, Louis P. Herzberg, Registration No. 41,500, Kevin M. Jordan, Registration No.40,277, Stephen C. Kaufman, Registration No.29,551, Daniel P. Morris, Registration No.32,053, Louis J. Percello, Registration No.33,206, Jay P. Sbrollini, Registration No. 36,266, David M. Shofi, Registration No. 39,835, Paul J. Otterstedt, Registration No. 37,411 and Robert M. Trepp, Registration No. 25,933, to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith.

Send all correspondence to: **McGinn & Gibb, P.C., 1701 Clarendon Boulevard, Suite 100, Arlington, Virginia 22209. Customer No. 21254**

Telephone calls should be directed to Sean M. McGinn, McGinn & Gibb, P.C. at (703) 294-6699.

(1) Inventor: Guy M. Cohen

Signature: Guy Cohen Date: 6/23/2000

Residence: 157 New Chalet Drive, Mohegan Lake, New York 10547

Citizenship: Israeli

Post Office Address: Same as Residence

(2) Inventor: Hon-Sum P. Wong

Signature: ______________________________ Date: ______________

Residence: 15 Valley View Road, Chappaqua, New York 10514

Citizenship: USA

Post Office Address: Same as Residence

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SYSTEM-ALIGNED GATE MOSFET WITH SEPARATE GATES

the specification of which:
(check one)

☒ is attached hereto.
☐ was filed on __________________, as Application Serial No. _________________ and was amended on __________.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

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Prior U.S. Applications:

Serial No.	Filing Date	Status
00/__________	May 15, 2000	Pending

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Tide 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: We hereby appoint Manny Schecter, Registration No.31,722, Lauren Bruzzone, Registration No. 35,082, Christopher A. Hughes, Registration No. 26,914, Edward A. Pennington, Registration No. 32,588, John E. Hoel, Registration No. 26,279, Joseph C. Redmond, Jr., Registration No. 18,753, Douglas W. Cameron, Registration No. 31,596, Louis P. Herzberg, Registration No. 41,500, Kevin M. Jordan, Registration No.40,277, Stephen C. Kaufman, Registration No.29,551, Daniel P. Morris, Registration No.32,053, Louis J. Percello, Registration No.33,206, Jay P Sbrollini, Registration No. 36,266, David M. Shofi, Registration No. 39,835, Paul J. Otterstedt, Registration No. 37,411 and Robert M. Trepp, Registration No. 25,933, to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith.

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